GE Fanuc Automation

Programmable Control Products

Series 90™ -70
High Speed Counter

User's Manual

GFK-1062A *November 1995*

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Preface

This manual provides the specifications, hardware interface requirements, and programming information needed to install and use the High Speed Counter module for the Series 90™-70 Programmable Logic Controller. The *Series 90-70 Programmable Controller Installation Manual*, GFK-0262, should be your primary reference for information about the Series 90-70 Programmable Logic Controller. It describes types of systems, system planning, installation procedures, and system components for the Series 90-70 PLC. Note that the High Speed Counter requires Logicmaster 90-70 release 5.0, or later.

Compatibility Requirements

The compatibility requirements for Series 90-70 CPU models and Logicmaster 90-70 programming software that are required for operation with the High Speed Counter are listed in the following table.

Product	Required Version
Series 90-70 CPU	5.03 or later (Models 731, 732, 771, 772) 5.50 or later (Adds Models 781, 782, 914, 924) 6.00 or later (Adds Models 915, 925)
Logicmaster 90-70 Programming Software	5.0x or later

Revisions to This Manual

This version of the Series 90-70 High Speed Counter User's Manual includes some additions and several corrections to the manual. These changes as compared to the previous version are listed below.

- Page 1-4, deleted reference to Hand-Held Programmer at end of third paragraph.
- Page 1-7, deleted sentence beginning with *Each output . . .* at end of first paragraph under **Outputs**.
- Page 3-14, added Error Code 31 to table at top of page.
- Page 4-4, deleted last two sentences in second paragraph under **Strobe Linkage.** Added third paragraph, beginning with *The following illustration . .* and added the following illustration and sentence after the illustration.
- Page 4-16, added Error Code 31 to table at top of page.
- Page 5-2, added statement at end of first sentence beginning with *that can be . . . .*
- Page 5-5, added heading *Differential Counting* and following illustrations.
- Page 5-18, added Error Code 31 to table.
- Page 6-15, added Error Code 31 to table at bottom of page.
- Page 7-4, added new paragraph beginning with *At power-up . . .* at top of page.

- Page 7-6, change wording of first two paragraphs under **Preset Outputs (Standard)**.
- Page 7-9, changed Output Mode Default entry in table to *Pulse*, and added a third value, *DISABLE*, for Preset CTR#.
- Page 7-16, added Error Code 31 to table (Error Codes for Type E Counter).
- Page 7-20, Changed heading beginning with **Preset Accumulator . . .** to read **Preset Accumulator (0, 1, or 2, presets 3 and 4 only)**, and added sentence under that heading beginning with *A data value . . .*
- Page C-5, added Error Descriptor 3 under *Nibble 1*.
- Page D-2, deleted environmental and general specifications from table and added reference to GFK-0867B after table.
- Page E-9, E-10, added description of application - *Measuring or Comparing Pulse Rates.*

Content of this Manual

This manual contains the following information:

Chapter 1. Introduction: provides an overview of the Series 90-70 High Speed Counter module features.

Chapter 2. Installation and Wiring: describes installation and field wiring for the High Speed Counter module.

Chapter 3. Counter Type A: describes operation of the Type A counter.

Chapter 4. Counter Type B: describes operation of the Type B counter.

Chapter 5. Counter Type C: describes operation of the Type C counter.

Chapter 6. Counter Type D: describes operation of the Type D counter.

Chapter 7. Counter Type E: describes operation of the Type E counter.

Appendix A. Using Special CPU Communications Functions: provides descriptions and examples of sending data commands to the High Speed Counter using the COMMREQ function in the PLC's ladder diagram and using the DOIO function as it relates to the High Speed Counter.

Appendix B. Using Interrupts with the HSC: provides a description of how to use interrupts with the High Speed Counter,

Appendix C. High Speed Counter Summary: provides a summary of return data, output data, data commands, error codes, and wiring information for the High Speed Counter.

Appendix D. Module Specifications: provides specifications for the High Speed Counter.

Appendix E. Application Examples: provides a group of application examples using the various features of the High Speed Counter.

Related Publications:

- *GFK-0262: Series 90™-70 Programmable Controller Installation Manual.* Describes system hardware components and system configuration, and provides installation and field wiring information for system planning and actual installation.
- *GFK-0401: Workmaster® II PLC Programming Unit Guide to Operation.* Describes installation and operation of the Workmaster II computer, specifically when it is used as the programming device for a Series 90 Programmable Logic Controller.
- *GFK-0263: Logicmaster™ 90-70 Programming Software User's Manual.* Explains use of Logicmaster™ 90-70 software to configure a Series 90-70 Programmable Logic Controller and create application programs.
- *GFK-0265: Series 90™-70 Programmable Controllers Reference Manual.* Describes the programming instructions used to create application programs for the Series 90-70 Programmable Logic Controllers.
- *GFK-1179: Installation Requirements for Conformance to Standards.* Describes installation requirements for programmable control products used in industrial environments, specifically, in situations where compliance to standards or directives from the Federal Communications Commission, the Canadian Department of Communications, or the European Union is necessary.

We Welcome Your Comments and Suggestions

At GE Fanuc Automation, we strive to produce quality documentation. After you have used this manual, please take a few moments to complete and return the Reader's Comment Card located on the next page.

Henry A. Konat
Senior Technical Writer

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Chapter 1 Introduction

This chapter describes:

- The High Speed Counter Module
- Configurable counter types
- Basic module features
- The module's inputs and outputs

High Speed Counter Module

The High Speed Counter (HSC) module, catalog number IC697HSC700, for the Series 90™-70 Programmable Logic Controller (PLC) provides direct processing of rapid pulse signals up to 200 kHz (800 kHz for Type E in A Quad B mode) for industrial control applications such as:

- Turbine flowmeter
- Meter proving
- Velocity measurement
- Material handling
- Motion control
- Process control
- Printing processes

Direct processing means that the module is able to sense inputs, process the input count information, and control the outputs without needing to communicate with a CPU.

The High Speed Counter uses 18 words of input memory. This consists of 32 bits of discrete input memory (%I) and 16 words of analog input memory (%AI). These inputs are updated once per CPU sweep. The High Speed Counter also uses 32 bits of discrete output memory (%Q) and 6 words of analog output memory (%AQ) which are transferred once per sweep. DOIO functions can be used to update any type of the HSC reference data more frequently.

The High Speed Counter is configured using the Logicmaster™ 90-70 Programming Software Configurator function. Many features can be configured from the user's application program as well. Each feature is set to a factory default configuration which is suitable for many applications. There are no jumpers or DIP switches to set on the module. The green LEDs at the top of the module indicate the operating status of the module and the current status of each of the preset outputs.

Configurable Counter Types

When the module is configured, a counter type must first be selected. The choices are:

- Type A - selects four identical, independent simple 16-bit counters
- Type B - selects two identical, independent 32-bit bidirectional counters
- Type C - selects one complex counter
- Type D - selects four identical, independent simple 32-bit counters
- Type E - selects two identical, fast response 16-bit counters

Type A Configuration

When used in this basic configuration, Type A, the module has four identical programmable up or down 16-bit counters. Each counter can be programmed to count either up or down. Each has three inputs: a Preload input, a Count Pulse input, and a Strobe input.

Type B Configuration

In its Type B configuration, the module has two identical bidirectional 32-bit counters. The count inputs may be configured to accept Up / Down, Pulse / Direction, or A Quad B signals. For a Type B counter configuration, each counter has two completely independent sets of Strobe inputs and Strobe registers. A Disable input is available to suspend counting. A Linked Strobe mode allows counter 2 counts to generate a strobe on both counters. This allows timing of a pulse by comparison to a known pulse rate.

Type C Configuration

In the Type C configuration, the module has one 32-bit counter with three strobe registers with strobe inputs, and two Preload values with Preload inputs. In addition, the module has a Home Position register for preloading the Accumulator to the Home Position value. Two sets of bi-directional counter inputs can be connected to operate in a differential fashion. Each set of inputs can be configured for A Quad B, Up / Down, or Pulse / Direction operation. The Type C configuration is suitable for applications requiring motion control, differential counting, or homing capability.

Type D Configuration

The Type D counter contains four identical 32-bit bidirectional counters which can interpret A Quad B, Up / Down, or Pulse / Direction inputs. A Home Position register allows a marker input to preload the Accumulator to the Home Position during a Home cycle. In A Quad B mode, the counter detects quadrature errors.

Type E Configuration

The Type E counter contains two identical 16-bit counters with Strobe and Preload inputs capable of counting Up / Down or A Quad B signals. Each has a Count Disable and a Strobe Disable input. The Type E counter is designed primarily as a Down counter, but can handle up counts to account for A Quad B *jitter*. When a counter counts down to zero, it turns on a dedicated preset output with a 15µs response time.

Description of Module

Module features include:

- 12 differential or single-ended (source) inputs with input voltage range selection of either 5 VDC (TTL) or 10 to 30 VDC (NON-TTL)

- 4 positive logic (source) outputs independently assignable to any available counter (Types A - D)
- External oscillator
- Built-in +5 VDC output
- Counts per timebase register for each counter (Types A - D)
- Software configuration
- Internal module diagnostics
- Individual LEDs that provide a visual indication of Module OK and Output States
- A removable terminal board for connection of field wiring

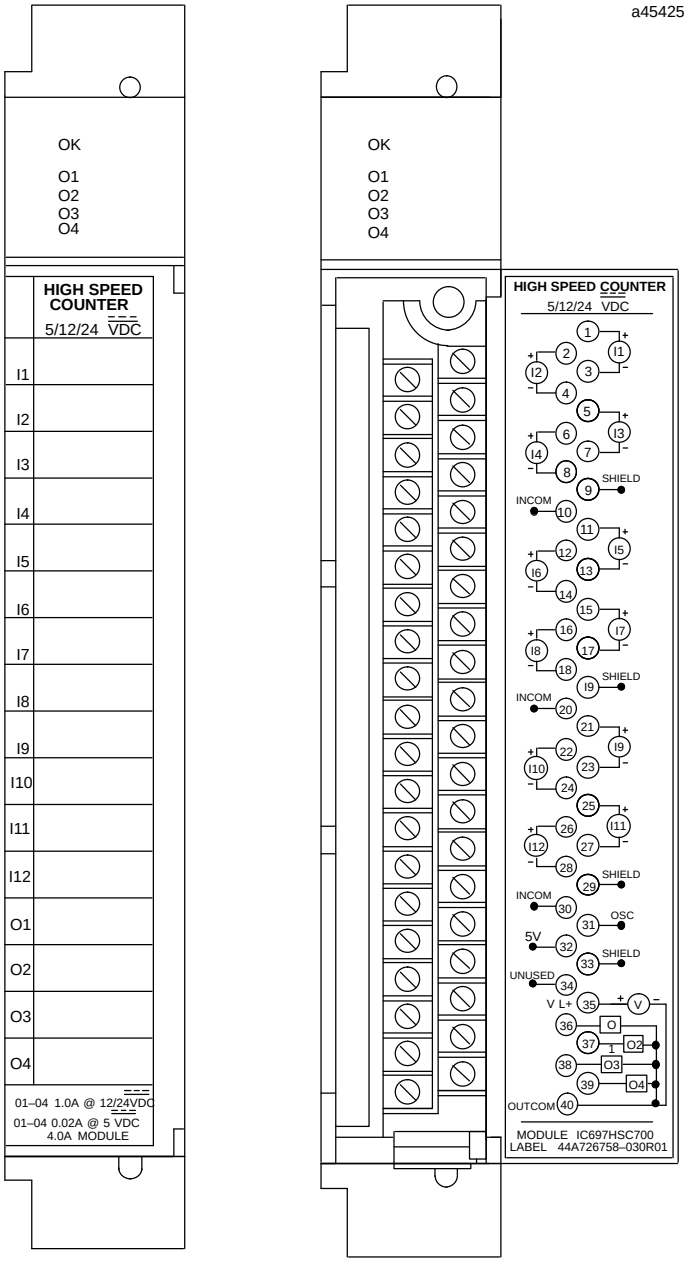


Figure 1-1. Series 90-70 High Speed Counter Module

Inputs can be used as count signals, direction, disable, edge-sensitive strobe, and preload inputs depending on the counter type selected by the user. Outputs can be used to drive indicating lights, solenoids, relays, and other devices.

For each counter, a Counts per Timebase register indicates the number of counts in a given time interval. The Counts per Timebase data is a 16-bit signed number. The sign indicates up counts (+) or down counts (–). The Timebase value is specified in milliseconds and ranges from 1 to 65535 milliseconds.

All configuration parameters for the module are downloaded from the PLC to the High Speed Counter after it passes its internal diagnostics and the MODULE OK indicator has turned on. An initial (default) set of configuration parameters is loaded during diagnostics. These default parameters can be used or modified through a download from the PLC.

Operation of the High Speed Counter module is monitored by a watchdog timer circuit which, if it detects a module failure, will force all outputs off and turn off the MODULE OK LED.

Type A, B, C, and D Operating Features

Operating features of the High Speed Counter for Types A, B, C, and D are described below. Features that have selectable parameters are configured using the Logicmaster 90 Programming Software Configurator function that has been installed on your programming computer. For detailed information about selectable features, refer to the applicable chapter for each counter type in this manual.

Count Rate

Maximum count rates are 200 KHz with the high frequency filter and 30 Hz with the low-frequency filter.

Selectable Input Filters

The Count, Count Disable, and Preload inputs for each counter can be configured for a high frequency filter (2.5 microseconds) or a low-frequency filter (12.5 milliseconds).

Continuous or Single-Shot Counting

Each counter can be configured to operate in either continuous or single-shot mode.

Continuous Counter Mode: If either the upper or lower count limit is exceeded the counter wraps around to the other limit and continues.

Single-shot Counter Mode: The counter counts to either the upper or lower limit and stops. When the counter is at the limit, counts in the opposite direction back it off from the limit.

Counter Accumulator

The Accumulator contains the current count value of each counter. The CPU can read the accumulator value or set it from the application program.

Counts per Timebase Register

Each counter stores the number of counts that have occurred in a specified period of time. A timebase value from 1 ms to 65535 ms can be configured.

Strobe Register

Type A, B and C counters have one or more Strobe registers that capture the current Accumulator value when a Strobe input transitions. The Strobe inputs are edge-triggered and can be configured for positive-edge or negative-edge response. The Strobe registers can be configured to update at any Strobe trigger or only on the first strobe trigger

Preloads

Counters A, B and C have one or more Preload inputs. The Preload inputs set the accumulator to a configured Preload value. %Q bits sent from the PLC can also be used to generate Preloads and set the accumulator to the configured Preload value.

Selectable On/Off Output Presets

Counter output signals can be configured to be On or Off when the count Accumulator reaches configured On and Off Preset values. There are four On / Off Preset outputs which can be independently assigned to any counter. An assigned output's state indicates when the counter Accumulator is between the defined On and Off points. Output polarity can be configured to On only between points or Off only between points by the relative location of the On / Off Presets.

Selectable Preset Interrupts

Each Preset output can generate PLC interrupts from On and / or Off transitions. Interrupts can be enabled for either or both transitions of each Preset output.

Oscillator

The module provides an external oscillator output that can be wired as a count input to any counter and used as a timing reference for measurement. The 5V square wave oscillator output can be configured to operate at frequencies from 15 Hz to 1 MHz. This output has a CMOS buffer with a 47 ohm output impedance.

Data Commands

The PLC can send data commands to the HSC70 through %AQ data or with a COMMREQ. These commands allow the user to dynamically modify counter operation and configuration parameters. Configuration parameters that can be dynamically modified include: accumulator value, counter limits, Preload values, On and Off Preset values and Home Position.

Velocity Command

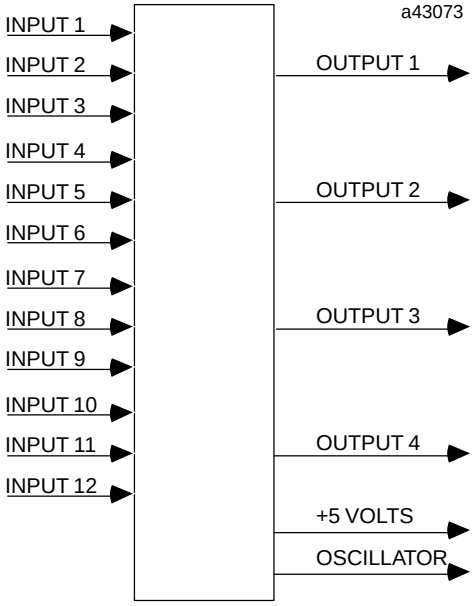
A %AQ or COMMREQ Data Command can be used to generate an internal velocity of up to 100,000 counts per second. The counter accumulator will increment or decrement at the commanded velocity. Counts generated by the user count inputs will be accumulated in addition to the Velocity Command counts.

Accumulator Adjust

A data command can be used to adjust the accumulator value from –128 to +127 counts at any time.

Module Inputs and Outputs

The High Speed Counter Module accepts 12 input signals, and can provide four output signals, plus an oscillator output and a +5 VDC output.



Inputs

Inputs can include count signals, Disable, edge-sensitive Strobe, and other inputs which can be configured for the application. Input filters can be configured for high frequency or low frequency operation.

Count Inputs:

A rising edge on a count input will increment or decrement its Count Accumulator. The method of counting depends upon the counter type and the count mode configured.

The Count input is positive-edge sensitive. It may be configured to have either the high-frequency (2.5mS) or low-frequency filter (12.5mS). The default filter is high-frequency.

Preload Inputs:

Each counter has a configurable preload register. The contents of this register determine the value the counter resets to when the Preload input goes active. The default value of the Preload register is zero.

The Preload input is positive-edge sensitive. It may be configured to have either the high-frequency (2.5mS) or low-frequency filter (12.5mS). The default is high-frequency.

If Preload occurs during counting, preload data with a resolution of Ç 1 count is stored in the accumulator and a Preload flag is set to indicate to the CPU that a Preload occurred.

Strobe Inputs:

Strobe inputs are edge-sensitive. They may be configured to respond to either the positive or negative edge. Strobe inputs always have the 2.5mS high-frequency filter enabled. On counter types with multiple strobe inputs, the strobes may occur simultaneously without affecting the integrity of the data strobed. When the strobe signal goes active, count data with a resolution of one count is stored in the associated Strobe register and a Strobe flag is set to indicate to the CPU that a strobe value was captured. ***This value remains in the Strobe register until the Strobe signal goes active again, at which time it is overwritten.*** Each time the CPU acknowledges receipt of the Strobe flag, the application program should clear it.

If a Strobe input and Preload input both go active in the same 0.5mS interval, both the Accumulator and Strobe register will be set to the Preload value.

Other Inputs:

These are described under the discussion of operation for each counter type.

Outputs

The module's four outputs can be used to drive indicating lights, solenoids, relays, and other devices. The outputs are also capable of driving CMOS level loads. Each output is a positive logic (source) output, with power supplied from a user supplied power source. The outputs are protected against short circuits by a common 3 Amp picofuse. Diodes protect outputs against transients going below output common.

The module's outputs can be programmed to turn on or off when the accumulated count reaches appropriate values. The count input-to-output delay is 1mS maximum (200mS minimum) plus the configured Input Filter Time.

Type E Operating Features

Operating features of the High Speed Counter for Type E are described below.

Count Rate and Input Filters

The maximum count rate with the low-frequency filter (12.5 milliseconds) is 30 Hz; with the high-frequency filter (2.5µs), the maximums are 200 KHz in Up / Down mode and 800 kHz in A Quad B mode. The Count, Count Disable, and Preload inputs for each counter can use either filter, but the Strobe and Strobe Disable inputs use only the high-frequency filter.

Continuous or Single-Shot Counting

Each counter can be configured to operate in either continuous or single-shot mode.

Continuous Counter Mode: When the counter decrements to zero, it turns on the fast response output and automatically preloads itself to the preload value and continues counting.

Single-shot Counter Mode: When the counter counts to zero, it turns on the fast response output and ignores count pulses until a preload occurs.

Preloads

A rising edge on the Preload input, a rising edge on the %Q Preload Accumulator bit, or the counter decrementing to zero in Continuous mode will set the accumulator to a configured Preload value. Preloads caused by the Preload input and count decrementing to zero will set a %I bit in the PLC to indicate a preload occurred.

Strobe Register Stack

Each counter has a Strobe Register stack which will store up to four strobe values. Strobes can be configured to occur on rising, falling, or both edges of the Strobe input. %I bits indicate how many strobes have occurred. A Reset Strobes %Q bit or a Preload clears the Strobe Register stack and %I indicators. A Strobe Disable input causes all Strobe input transitions to be ignored.

Counter Outputs

The Type E counter supports two types of output presets, Fast Response and Standard.

Fast Response: There is one dedicated fast response output for each accumulator. The fast response output turns on within 15µs of the associated counter decrementing to zero, with less than 2µs variation. In addition, two output modes are supported for the fast response outputs.

Pulse Output Mode: The output turns on when the Accumulator counts down to zero and stays on for a configured duration, from 1 to 1000 milliseconds.

Latched Output Mode: (Single Shot mode only) The output turns on when the Accumulator counts down to zero and stays on until a Preload occurs.

Standard Output Presets: Outputs 3 and 4 can be assigned to either counter and configured to be On or Off when the count Accumulator reaches configured On and Off values. An assigned output's state indicates when the counter Accumulator is between the defined On and Off points.

Output Interrupts

Interrupts can be enabled or disabled for Off to On transitions of the fast response outputs. Interrupts can be enabled or disabled for either transition of the standard preset outputs.

Oscillator

The module provides an external oscillator output that can be wired as a count input to any counter and used as a timing reference for measurement. The 5V square wave oscillator output can be configured to operate at frequencies from 15 Hz to 1 MHz. This output has a CMOS buffer with a 47 ohm output impedance.

Data Commands

The PLC can send data commands to the HSC70 through %AQ data or with a COMMREQ. These commands allow the user to dynamically modify counter operation and configuration parameters. Configuration parameters that can be dynamically modified include: Preload values, On and Off Preset values, and Fast Response output duration.

Chapter 2

Installation and Wiring

I/O Module Installation and Wiring

This chapter contains information on installing the High Speed Counter module and information relevant to field wiring to and from the module.

Recommended Field Wiring Procedures

The following procedures are recommended when connecting field wiring to the detachable terminal board on the module. Module features referenced in the following procedures that are common to all Series 90-70 I/O modules are shown in the following figure.

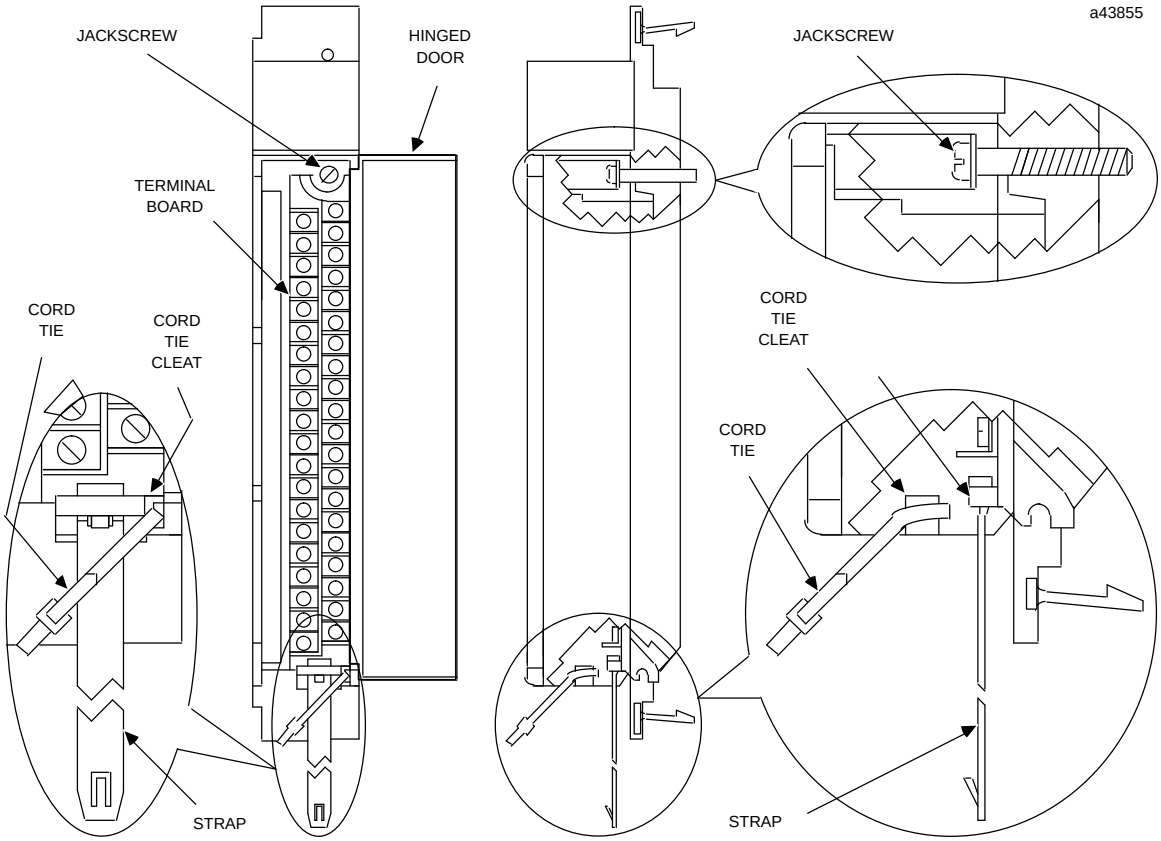


Figure 2-1. I/O Module Features

1. Turn off power before removing or installing terminal boards. Open the hinged door on the module to access a jackscrew which holds the terminal board securely in place. The detachable field wiring terminal board can now be removed from the module by turning the jackscrew counter-clockwise until it is fully disengaged.
2. To remove the terminal board, grasp the top of the terminal board and swing it outward.

Caution

Do not use the hinged door to remove the terminal board. The hinged door could be damaged if this is done.

3. The terminal board is designed to accept wire sizes from AWG #22 (0.35 mm^2) through AWG #14 (2.1 mm^2). It is important that when using AWG #14 (2.1 mm^2) wire for wiring all points, that a maximum insulation diameter of .135 inch (3.43 mm) not be exceeded. To ensure proper connection, two wires may be terminated on any one terminal only if both wires are the same size.
4. The terminal board is designed to accept a maximum of (40) AWG #14 (2.1 mm^2)wires. If AWG #14 (2.1 mm^2) wires are to be used, then wire markers should be placed at least 8 inches (203 mm) from termination end to provide sufficient space for the hinged door to close.

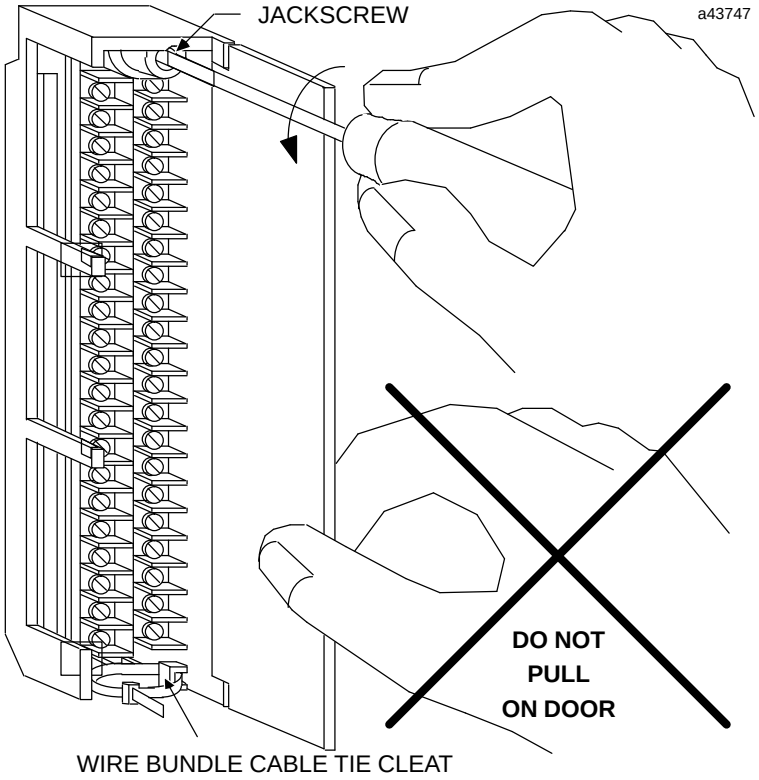


Figure 2-2. Removal of I/O Terminal Board

5. After completing connections to all modules in a rack, the wire bundle must be secured. To ensure that the wire bundle is secured properly, it is recommended that a cable tie be wrapped around the wire bundle and tightly secured through the cable tie cleat located

at the lower right corner of the terminal board. For extremely large wire bundles, additional cable ties should be used.

6. A door label insert is included with each module to indicate circuit wiring information and provide space to record user circuit wiring identification. A slot is provided on the hinged door to allow for insertion of this label. If the label is difficult to insert, crease the scored edge before insertion. The outside label has a color coded stripe to allow quick identification of the module voltage type (blue: low voltage; red: high voltage).
7. After field wiring is completed, the terminal board should be securely fastened to the rack by inserting the terminal board strap (attached to each module) into the small rectangular slots in the bottom card guide grill on the rack. This strap not only secures the terminal board to the rack, it also provides a way of identifying the wired terminal board with its correct mating rack slot location.
8. For adequate module ventilation, it is recommended that at least a 6 inch (152 mm) clearance be allowed above and below the rack grill. Wire bundles should not obstruct the rack grill work.

Removing an I/O Module

The instructions below should be followed when removing an I/O module from its slot in a rack.

- Grasp the board firmly at the top and bottom of the board cover with your thumbs on the front of the cover and your fingers on the plastic clips on the back of the cover.
- Squeeze the rack clips on the back of the cover with your fingers to disengage the clip from the rack rail and pull the board firmly to remove it from the backplane connector.
- Slide the board along the card guide and remove it from the rack.

Field Wiring Considerations

It is recommended that the following procedures be followed when routing and connecting field wiring from user devices to the PLC or to Output devices to be controlled by the PLC.

- All low level signal wires should be run separately from other field wiring.
- AC power wiring should be run separately from DC field wiring.

Warning

You should calculate the maximum current for each wire and observe proper wiring practices. Failure to do so may cause injury to personnel or damage to equipment.

- Field wiring should not be routed close to any device that could be a potential source of electrical interference.
- If severe noise problems are present, additional power supply filtering or an isolation transformer may be required.
- Ensure that proper grounding procedures, as previously described, are followed to minimize potential safety hazards to personnel.
- Label all wires to and from I/O devices. Record circuit identification numbers or other pertinent data on the inserts which go in the module's faceplate door.

Terminal Board Pin Assignments

The High Speed Counter Module has a removable terminal strip for connection to field devices. High Speed Counter terminal board pin assignments for field wiring connections are shown in the following figure.

The following figure provides wiring information for field connections to and from the High Speed Counter.

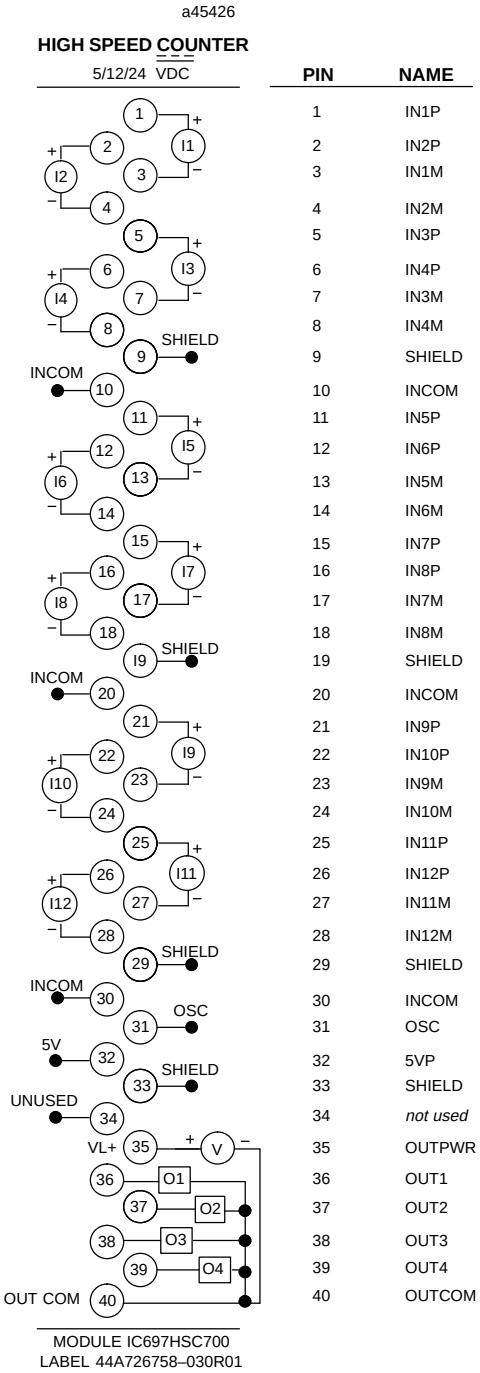


Figure 2-3. Field Wiring for the High Speed Counter

Note

All 12 High Speed Counter inputs are positive logic (source) type.

Transducers with CMOS buffer outputs (74HC04 equivalent) can directly drive the High Speed Counter inputs using the 5V input range.

Transducers using TTL totem pole or open collector outputs must include a 470 ohm pullup resistor (to 5V) to guarantee compatibility with the High Speed Counter inputs.

Transducers using high voltage open collector (sink) type outputs must have a 1K pullup resistor to +12V for compatibility with the High Speed Counter 10 to 30 volt input range.

Caution

Do not connect 10 to 30 VDC to the module inputs when the 5 VDC input range (pins 13 to 15 jumpered) is selected. Doing so will cause damage to the module.

Terminal Assignments for Counter Type

The following table defines which terminals to use for the type of counter selected during module configuration.

Table 2-1. Pin Assignments for Each Counter Type

Pin	Signal Name	Pin Definition	Signal Name by Counter Type				
			Type A	Type B	Type C	Type D	Type E
1	IN1P	Positive Logic Input - Positive	CH1P	CH1AP	CH1AP	CH1AP	CH1AP
2	IN2P	Positive Logic Input - Positive	CH2P	CH1BP	CH1BP	CH1BP	CH1BP
3	IN1M	Positive Logic Input - Negative	CH1M	CH1AM	CH1AM	CH1AM	CH1AM
4	IN2M	Positive Logic Input - Negative	CH2M	CH1BM	CH1BM	CH1BM	CH1BM
5	IN3P	Positive Logic Input - Positive	CH3P	CH2AP	CH2AP	CH2AP	CH2AP
6	IN4P	Positive Logic Input - Positive	CH4P	CH2BP	CH2BP	CH2BP	CH2BP
7	IN3M	Positive Logic Input - Negative	CH3M	CH2AM	CH2AM	CH2AM	CH2AM
8	IN4M	Positive Logic Input - Negative	CH4M	CH2BM	CH2BM	CH2BM	CH2BM
9	SHIELD	Cable Shield	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD
10	INCOM	Common for positive logic inputs	INCOM	INCOM	INCOM	INCOM	INCOM
11	IN5P	Positive Logic Input - Positive	PRLD1P	PRLD1P	PRLD1P	CH3AP	PRLD1P
12	IN6P	Positive Logic Input - Positive	PRLD2P	DISABLE1P	DISABLE1P	CH3AP	DISABLE1P
13	IN5M	Positive Logic Input - Negative	PRLD1M	PRLD1M	PRLD1M	CH3AM	PRLD1M
14	IN6M	Positive Logic Input - Negative	PRLD2M	DISABLE1M	DISABLE1M	CH3BM	DISABLE1M
15	IN7P	Positive Logic Input - Positive	PRLD3P	PRLD2P	PRLD2P	CH4AP	PRLD2P
16	IN8P	Positive Logic Input - Positive	PRLD4P	DISABLE2P	HOMEP	CH4BP	DISABLE2P
17	IN7M	Positive Logic Input - Negative	PRLD3M	PRLD2M	PRLD2M	CH4AM	PRLD2M
18	IN8M	Positive Logic Input - Negative	PRLD4M	DISABLE2M	HOMEM	CH4BM	DISABLE2M
19	SHIELD	Positive Logic Output	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD

Table 2-1. Pin Assignments for Each Counter Type (continued)

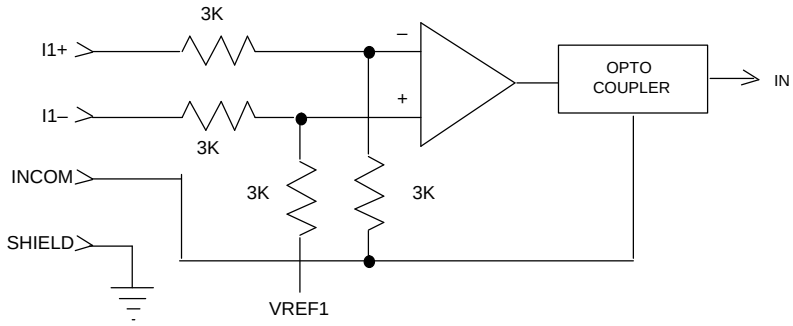
Pin	Signal Name	Pin Definition	Signal Name by Counter Type				
			Type A	Type B	Type C	Type D	Type E
20	INCOM	Common for positive logic inputs	INCOM	INCOM	INCOM	INCOM	INCOM
21	IN9P	Positive Logic Input - Positive	STRB1P	STRB11P	STRB11P	MRKR1P	STRB1P
22	IN10P	Positive Logic Input - Positive	STRB2P	STRB12P	STRB12P	MRKR2P	STRB2P
23	IN9M	Positive Logic Input - Negative	STRB1M	STRB11M	STRB11M	MRKR1M	STRB1M
24	IN10M	Positive Logic Input - Negative	STRB2M	STRB12M	STRB12M	MRKR2M	STRB2M
25	IN11P	Positive Logic Input - Positive	STRB3P	STRB21P	STRB21P	MRKR3P	STRBDIS1P
26	IN12P	Positive Logic Input - Positive	STRB4P	STRB22P	MRKR1P	MRKR4P	STRBDIS2P
27	IN11M	Positive Logic Input - Negative	STRB3M	STRB21M	STRB21M	MRKR3M	STRBDIS1M
28	IN12M	Positive Logic Input - Negative	STRB4M	STRB22M	MARK1M	MRKR4M	STRBDIS2M
29	SHIELD	Cable Shield	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD
30	INCOM	Common for positive logic inputs	INCOM	INCOM	INCOM	INCOM	INCOM
31	OSC	Oscillator Input	OSC	OSC	OSC	OSC	OSC
32	5VP	5 VDC Power Source	5VP	5VP	5VP	5VP	5VP
33	SHIELD	Cable Shield	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD
34	*SPARE*	*not used*	*SPARE*	*SPARE*	*SPARE*	*SPARE*	*SPARE*
35	OUTPWR	Common for outputs	OUTPWR	OUTPWR	OUTPWR	OUTPWR	OUTPWR
36	OUT1	Output 1, PositiveLogic	HSCOUT1	HSCOUT1	HSCOUT1	HSCOUT1	HSCOUT1
37	OUT2	Output 2, PositiveLogic	HSCOUT2	HSCOUT2	HSCOUT2	HSCOUT2	HSCOUT2
38	OUT3	Output 3, PositiveLogic	HSCOUT3	HSCOUT3	HSCOUT3	HSCOUT3	HSCOUT3
39	OUT4	Output 4, PositiveLogic	HSCOUT4	HSCOUT4	HSCOUT4	HSCOUT4	HSCOUT4
40	OUTCOM	Common for outputs	OUTCOM	OUTCOM	OUTCOM	OUTCOM	OUTCOM

User Inputs

- *Input Type:* Differential or single-ended, optically isolated
- *Input Range:* TTL, Non-TTL, or Magnetic Pickup
- *Input Impedance:* 6000 W
- *Input Filtering:* 10 ms to 2 ms selectable
- *Input Hysteresis:* 250 mV, typical
- *Input Cable*: Shielded cable is recommended with maximum length of 30 meters (100 Feet)

Typical User Input Circuit Diagram

a47070

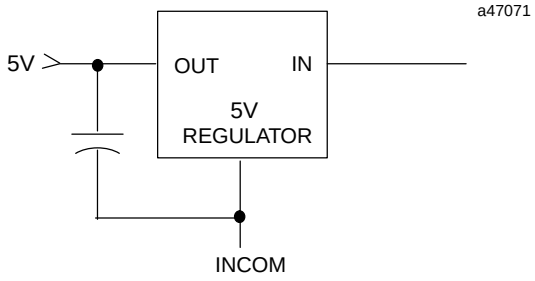


Encoder Installation

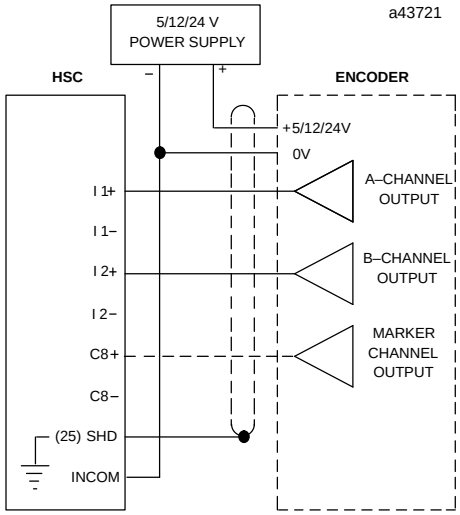
- *Encoder Power:* Optically isolated current limited +5 Volt supply is available at the High Speed Counter I/O connector. Maximum load should be 500 mA at 40°C (104°F) or 300 mA at 60°C (140°F).
- *Encoder Common:* INCOM (same as User Inputs)
- *Quadrature Tolerance:* 90 degrees Ç 45 degrees
- *Z (Marker) Channel:* Positive edge triggered. Minimum pulse width 4 ms.
- *Encoder Direction of Travel:* Channel A leading Channel B indicates positive direction.

Encoder Power Circuit Diagram

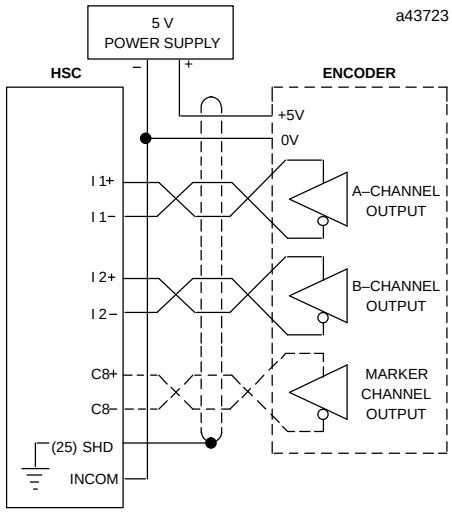
a47071



Typical Encoder Connections Using External Power Supply



Connections for Single-Ended Inputs Power: Positive Loop

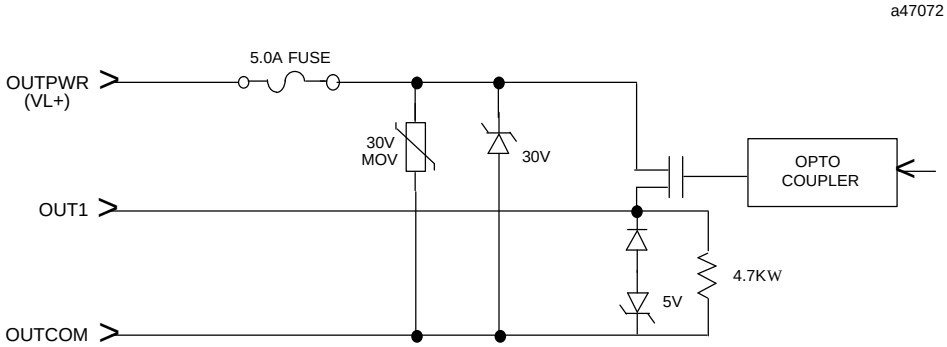


Connections for Differential Inputs Power: Positive Loop

User Outputs

- *Output Type:* Positive logic, optically isolated
- *Output Supply Voltage:* 30.0 VDC
- *Maximum Load Current:* 1.0 A for each output using 10 to 30 VDC supply
- *Typical 5 VDC Output Current:* 20 mA
- *Inductive Load Clamp Voltage:* –8.0 V typical
- *Off State Leakage Current*: 10 mA per output
- *Typical Output Response Time:* 500 ms
- *Output protection:* Single 5.0 A, 5x20mm fuse

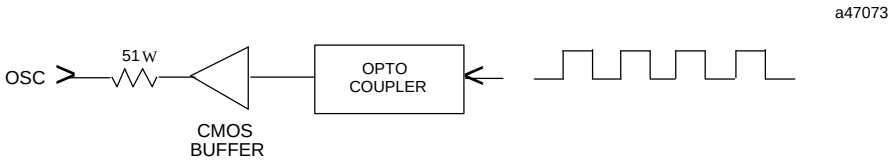
Typical Output Circuit



Oscillator Output

- *Output Type:* CMOS, optically isolated
- *Maximum Load Current:* 50 mA
- *Minimum High Level Output Voltage V_{OH} at 20 mA:* 3.7 V
- *Minimum Low Level Output Voltage V_{OL} at 20 mA:* 0.2 V
- *Oscillator Common:* INCOM (shared with User Inputs)

Oscillator Output Circuit

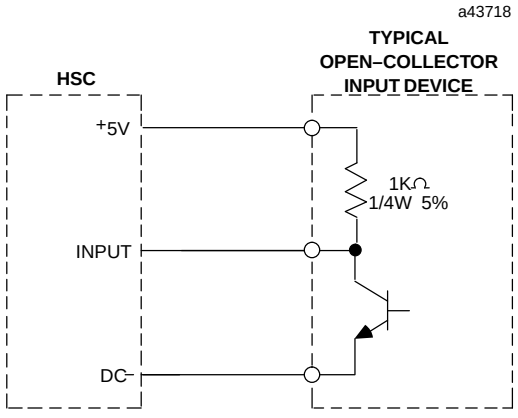


Wiring for TTL Open-Collector Input Devices

For TTL open-collector inputs, an external resistor must be provided. Be sure the input device is capable of handling the load current represented by the suggested resistor value.

Open-collector Input Device with +5 Volt Power Provided by the High Speed Counter

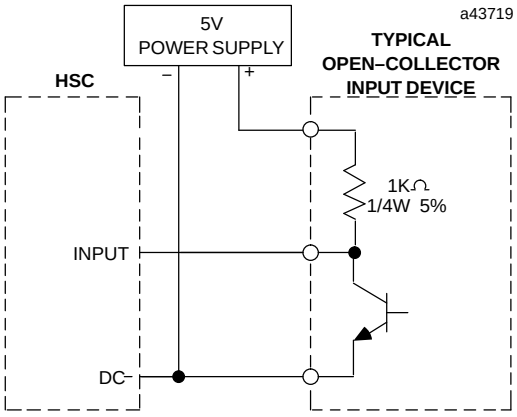
When using +5 volt power provided by the High Speed Counter, use a nominal pullup resistor of 1K ohm, 1/4 Watt, 5%.



Open-collector Input Device with External Power Supply

For an external power supply, suggested nominal resistors are:

- 1K ohm, 1/4 Watt, 5% for a +5 volt supply.
- 1.5K ohm, 1/4 Watt, 5% for a +12 volt supply.
- 4.7K ohm, 1/4 Watt, 5% for a +24 volt supply.



Chapter 3 Counter Type A

Counter Type A is described in this chapter. The description includes counter operation, configuration of the counter, and the interface between the counter and CPU.

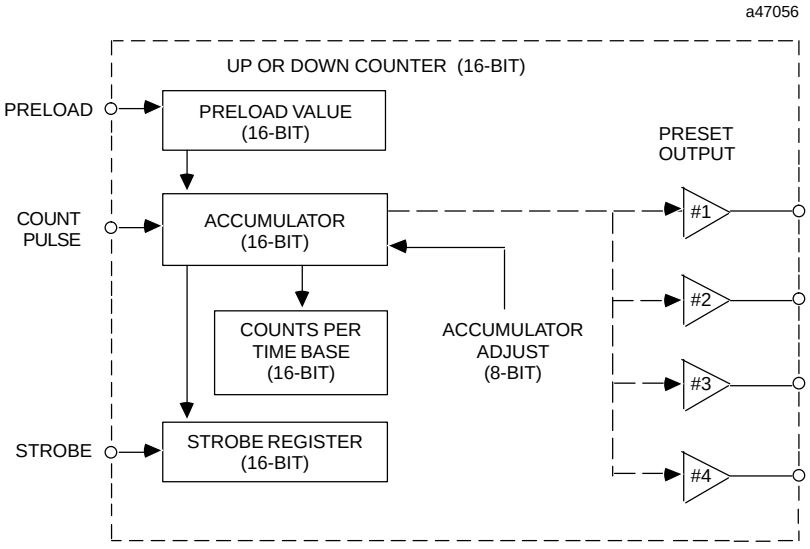
Contents and Operation of a Type A Counter

Overview

The Series 90-70 High Speed Counter, when configured as Type A contains four 16-bit unidirectional counters. Each counter is controlled by 3 of the 12 single ended or differential voltage inputs: Count Pulse, Strobe, and Preload. Each counter can be individually configured to count either up or down. Counter Type A elements are shown in the figure below. Each counter has the following:

- accumulator register which counts the pulses on the Count Pulse input
- a strobe register which stores the accumulator value when the Strobe input transitions
- a preload value which is inserted into the accumulator when a preload occurs
- a counts per timebase register which indicates the count rate of the Count Pulse input pulses.

Each of the four 5 to 30 V preset outputs can be independently assigned to any of the four counters, and can be used to generate PLC interrupts.



Count Pulse Input and Accumulator

Positive transitions on the Count Pulse input will increment or decrement the 16-bit Accumulator value by one count depending on the counter direction. The counter direction is initially set in the configuration, and may be changed by using a data command.

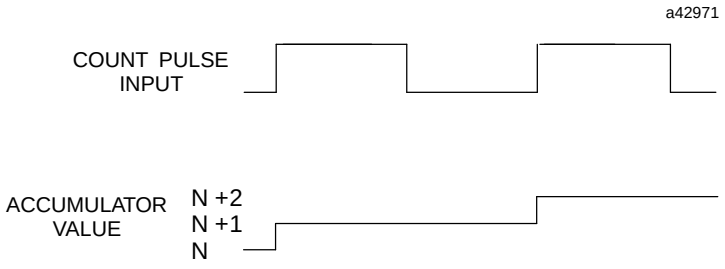
The Accumulator is bounded by configurable High and Low Limits. The interaction between the Accumulator and the limits depends on the configured count mode. In *Continuous mode*, the Accumulator will increment or decrement to the current High or Low Limit, roll over to the other limit, and continue counting. In *Single Shot* mode, the Accumulator will count to the current High or Low Limit and stop. If the counter direction is changed, the Accumulator will count away from the limit until it reaches the other limit.

The High and Low Limits can be changed to any valid 16-bit value at any time using a data command from the PLC. To be a valid 16-bit value, the following conditions must be met:

- the High Limit must be greater than the Low Limit
- the Preload value must be within the High and Low Limit bounds
- any presets assigned to the counter must have ON and OFF values within the High and Low Limit bounds.

If the limits are changed so the Accumulator is outside the limit boundaries, the Accumulator is set to the Low Limit.

The Accumulator can be set to any 16-bit value within the bounds of the High and Low limits at any time using a data command. Another data command allows the Accumulator to be adjusted by a byte increment value, from –128 to +127 counts. Finally, a velocity can be commanded which causes the Accumulator to increment or decrement at a fixed rate. The following figure illustrates the counting operation and timing of a counter counting up.



Strobe Input and Register

The Strobe input is an edge sensitive input which can be configured to respond to either a positive edge or a negative edge. When the configured Strobe input transition occurs, (referred to as a Strobe Pulse) the value in the Accumulator is stored in the Strobe register and a strobe flag is set and returned in %I data to indicate the event to the CPU. The application program in the CPU acknowledges receipt of the strobe by toggling the corresponding Strobe Status %Q bit.

Two strobe modes are available to select which Strobe value is most important. **In *Last Strobe* mode (the default) a Strobe Pulse will always update the Strobe register with**

the latest Accumulator value regardless of the strobe status flags. In First Strobe mode, the first strobe is captured and all subsequent Strobe Pulses are ignored until the strobe flag is cleared by toggling the corresponding Reset Strobe %Q bit.

The Strobe then Preload configuration option allows a Strobe Pulse to, in addition to capturing the Accumulator value in the Strobe register, automatically perform a preload by placing the configured preload value into the Accumulator and setting the preload flag in the %I data.

Preloads

Preloads are normally used to perform a reset function for the counter. The value to which the Accumulator is set when a preload occurs can be configured to any 16-bit value within the range of the High and Low Limits and has a default value of zero. The Preload value can also be changed using a data command from the PLC. There are two types of Preloads, hardware and software.

A hardware preload uses the Preload input and is positive edge sensitive only. On the positive transition, the configured Preload value is inserted into the Accumulator and the Preload flag is set and returned in %I data to indicate the event to the CPU. If an application program uses this status flag, it may use the corresponding %Q bit to clear the Preload flag before the next preload occurs. **A rising edge on the Preload input always preloads the Accumulator regardless of the state of the Preload flag.**

Note that when a pulse occurs on the Preload inputs at the same time that a Strobe pulse occurs, or if the inputs are tied together, the Preload has precedence. The Accumulator will be set to the Preload value and then the Strobe register will be set to the Accumulator. Thus the Strobe register will obtain a copy of the Preload value. The counter will automatically perform a Preload after every Strobe pulse when the Strobe Effect configuration option is set to Strobe then Preload.

A software preload can be performed by setting a Preload Accumulator %Q bit. On the positive transition of this %Q bit, the current preload value is placed into the Accumulator. A software preload does NOT set the Preload flag.

Counts per Timebase Register

The Counts per Timebase register is a 16-bit register which contains the number of counts received on the Count Pulse input in the last completed timebase interval. It is used to measure the rate of counting. If more counts are received than can be stored in a 16-bit register, the register will overflow. The timebase interval is a configurable value from 1 to 65535 milliseconds.

Changes to the timebase will not take effect until after the previous timebase and one new timebase have elapsed. A Preload will interrupt counting and cause the Counts per Timebase register to be inaccurate for up to two timebase intervals. The timebase is initially configured as 1 second, but may be changed using the Logicmaster 90-70 Configurator function or a data command.

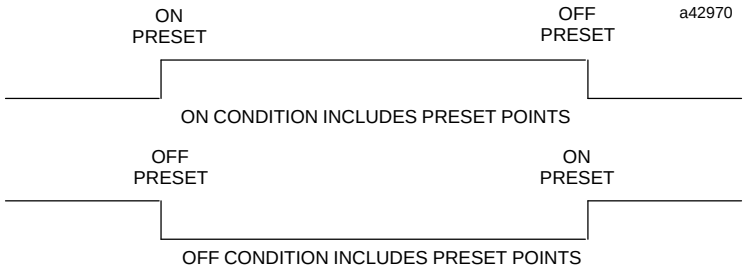
As an unsigned number, the Counts per Timebase register will correctly indicate from 0 to 65536 positive counts received per timebase. As a signed number, it will properly indicate from –32768 to 32767 counts per timebase. The timebase should be selected to not allow more counts in a timebase than the 16-bit register can hold or it will overflow.

Preset Outputs

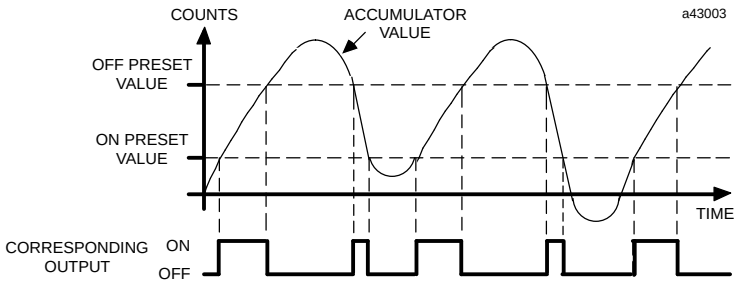
The module has four preset outputs, each of which can be assigned to any counter. Each preset output has a preset ON and preset OFF value, or position, which must be within the count limits of the counter to which the preset is assigned. The preset ON and OFF positions determine when the output will be ON or OFF, as shown below.

Preset closest to low limit	Output ON	Output OFF
ON	> = ON Preset < = OFF Preset	> OFF Preset < ON Preset
OFF	< OFF Preset > ON Preset	< = ON Preset > = OFF Preset

The output may be either on or off when the accumulator value lies between the Preset points.



For example:



Separation of Preset Points

The count accumulators are compared to the Presets at 0.5 msec intervals. Therefore, to guarantee that the outputs will always switch, the Preset points must be separated by at least the number of counts received in a 0.5 msec time period. For example:

If maximum count rate = 10kHz;
then minimum count separation = (10,000 Hz x .0005 sec) = 5 counts.

Preset Interrupts

Interrupts can be enabled or disabled for each preset output's ON and OFF transition. At the same time a preset output changes state, the CPU is interrupted. %I and %AI data is transferred so that the interrupt routine will see the most current data from the High Speed Counter. Simultaneous preset changes generate only one interrupt to the CPU, so the updated %I data must be used by an interrupt routine to determine which presets changed state and which edge(s) generated the interrupt. Once configured, interrupts can be independently enabled or disabled using data commands. See Appendix B for information on using the interrupt capability.

Output Failure Mode

When the CPU is stopped or lost, counter operation continues normally without interfacing to the CPU. Preset output operations during this stopped state can be configured for one of three modes. In Normal mode, the outputs continue to operate as if the CPU were present, changing state to reflect the counter Accumulators. In Force Off mode, all preset outputs are turned off and remain off until the CPU returns. In Holdlast mode, the preset outputs retain current levels and do not reflect the counter Accumulators. If the CPU resumes operation, the outputs will immediately begin reflecting the counter Accumulators.

Oscillator Output

The High Speed Counter module generates a 5V square wave oscillator signal. The oscillator output frequency is determined by the current oscillator divider (set in configuration or by data command) as indicated below:

Oscillator Frequency (Hz) = 1,000,000 Ï *oscillator div*ider

The output frequency ranges from approximately 15 Hz (oscillator divider of 65535) to 1 MHz (oscillator divider of 1).

Table 3-1. Type A Specific Terminal Strip Assignments

Pin	Signal Name	Type A Pin Name	Type A Pin Description
1,3	IN1	COUNT PULSE 1	Counter 1 count input
2,4	IN2	COUNT PULSE 2	Counter 2 count input
5,7	IN3	COUNT PULSE 3	Counter 3 count input
6,8	IN4	COUNT PULSE 4	Counter 4 count input
11,13	IN5	PRELOAD 1	Counter 1 preload input
12,14	IN6	PRELOAD 2	Counter 2 preload input
15,17	IN7	PRELOAD 3	Counter 3 preload input
16,18	IN8	PRELOAD 4	Counter 4 preload input
21,23	IN9	STROBE 1	Counter 1 strobe input
22,24	IN10	STROBE 2	Counter 2 strobe input
25,27	IN11	STROBE 3	Counter 3 strobe input
26,28	IN12	STROBE 4	Counter 4 strobe input

Configuring the Type A High Speed Counter

The following table summarizes all configuration features and default configuration values for the Type A counter.

Configuration Parameter	Description	Values	Default
Failure Mde	Output Failure Mode	NORMAL, OFF, HOLD	NORMAL
Osc Divider	Oscillator Divider	1 ... 65535	1000
Count Thrshlds	Count Input Thresholds	NON-TTL, TTL, MAG-PKUP	NON-TTL
Control Thrshlds	Control Input Thresholds	NON-TTL, TTL	NON-TTL
Count Filtr	Count Input Filter	HIFREQ, LOWFREQ	HIFREQ
Preld Filtr	Preload Input Filter	HIFREQ, LOWFREQ	HIFREQ
Preset CTR#	Preset Accumulator	CTR1 ... CTR4	Preset #
Preset ON	Preset ON setpoint	Low Limit ... High Limit	32767
Preset OFF	Preset OFF setpoint	Low Limit ... High Limit	0
ON Interrupt	Preset on transition interrupt	DISABLED, ENABLED	DISABLED
OFF Interrupt	Preset off transition interrupt	DISABLED, ENABLED	DISABLED
Hi Limit	High Count Limit	–32768 ... 32767	32767
Lo Limit	Low Count Limit	–32768 ... 32767	0
Count Mode	Count Mode	CONTINU, SINGSHOT	CONTINU
Count Dir	Count Direction	UP, DOWN	UP
Timebase(ms)	Timebase	1 ... 65535 ms	1000 ms
Preld Value	Preload Value	Low Limit ... High Limit	0
Strobe Mode	Strobe Mode	LAST, FIRST	LAST
Strobe Edge	Strobe Edge	POS, NEG	POS
Strobe Efct	Strobe Effect	STRB / PRELOAD, STRB ONLY	STRB ONLY

Output Failure Mode

When the CPU is stopped or lost, counter operation continues normally; however, the operation of the Preset outputs can be configured until the CPU returns or power is cycled. In all modes, the Accumulators are updated and the Strobes and Preloads are processed normally.

- In Normal mode (NORMAL), the outputs continue to operate as if the CPU were present. Outputs will change state to reflect the counter Accumulators.
- In Force Off mode (OFF), all preset outputs are turned off and remain off until the CPU returns.
- In Holdlast mode (HOLD), the preset outputs retain current levels and do not reflect the counter Accumulators.

If the CPU returns to operation or the module is power-cycled, the outputs will immediately begin reflecting the counter Accumulators again.

Oscillator Divider

The oscillator divider is used to generate a 5V oscillator output. The output frequency is 1 million divided by the oscillator divider; the formula is shown below.

Oscillator Frequency (Hz) = 1,000,000 / oscillator divider

The output frequency ranges from approximately 15 Hz (oscillator divider of 65535) to 1 MHz (oscillator divider of 1).

Input Thresholds

All inputs can be used as differential or single-ended inputs. The following table specifies the input thresholds for single-ended and differential use based on threshold selection and input type. The configuration parameters will set input thresholds according to the following table:

Configuration Parameter	Inputs Controlled	Input Definitions
Count 1, 2 Threshold	IN1, IN2	Count Pulse 1, 2
Count 3, 4 Threshold	IN3, IN4	Count Pulse 3, 4
Control 1, 2 Threshold	IN5, IN6, IN9, IN10	Preload and Strobe 1, 2
Control 3, 4 Threshold	IN7, IN8, IN11, IN12	Preload and Strobe 3, 4

Note that all the inputs controlled will have the same voltage threshold.

The voltage thresholds which can be selected for each input are described in the following table.

Input Type	Single-Ended			Differential		
	Non-TTL	TTL	Mag-Pickup	Non-TTL	TTL	Mag-Pickup
Counter 1, 2 Threshold	8 V	1.4 V	0.1 V	4.8 V	0.8 V	0.1 V
Counter 3, 4 Threshold	8 V	1.4 V	0.1V	4.8 V	0.8 V	0.1V
Control 1, 2 Threshold	8 V	1.4 V	X	4.8 V	0.8 V	X
Control 3, 4 Threshold	8 V	1.4 V	X	4.8 V	0.8 V	X

Input Filters

All inputs default to using a 2.5 microsecond high-frequency filter. Each Count Pulse and Preload input can be configured to use a 12.5 millisecond low-frequency filter instead. The low-frequency filter reduces the effects of signal noise. The Strobe inputs always use the high-frequency filter.

Preset Accumulator

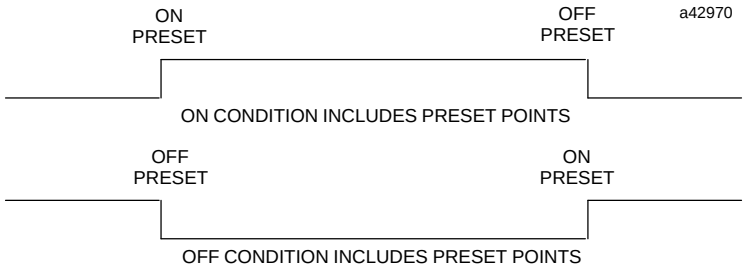
The Preset Accumulator field determines which counter a preset output will reflect. Each of the four preset outputs can be assigned to any of the accumulators. The Preset ON and Preset OFF values must be within the range of the High and Low Limits of the counter the Preset Accumulator is assigned to. The default for each Preset is to reflect the counter of the same number. Thus Preset 1 points to counter 1, Preset 2 points to counter 2, etc.

Output Preset ON and OFF Positions

Each preset output has a preset ON and OFF position. The output state reflects the counter accumulator value in relation to the ON and OFF points.

Preset closest to low limit	Output ON	Output OFF
ON	> = ON Preset < = OFF Preset	> OFF Preset < ON Preset
OFF	< OFF Preset > ON Preset	< = ON Preset > = OFF Preset

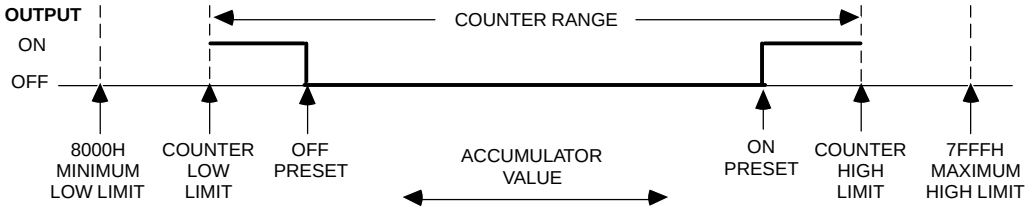
The output may be either on or off when the accumulator value lies between the Preset points.



Location of Preset Points

The Preset points may be located anywhere within the counter range. When the accumulator value is between the Preset points, the output ON / OFF state will always be that of the lowest (most negative) Preset point. When the accumulator value is *not* between the Preset points, the output ON / OFF state will be that of the most positive preset. This is true regardless of the counter direction.

The following example compares the output state and accumulator value of a 16-bit counter when the OFF Preset value is closer to the Low Limit than the ON Preset value,



Preset Interrupt Enables

Each preset can generate an interrupt to the CPU. If the Interrupt ON selection is enabled, then an ON transition of the preset output will generate an interrupt to the CPU. Similarly, if the Interrupt OFF selection is enabled, an OFF transition of the preset output will generate an interrupt to the CPU. Thus no edge, either edge, or both edges of a preset output transition can generate an interrupt. The default is for all interrupts to be disabled.

Count Limits

Each counter is assigned upper and lower count limits. The upper (high) limit must be the most positive, and the lower limit must be the most negative. Both limits can be positive or negative, but the high limit must always be greater than the low limit. A counter's Accumulator, Preload value, and any Preset outputs assigned to the counter must lie within the high and low limits.

If the Accumulator value is outside the new limits when the limits are changed, it is automatically adjusted to the low limit value. If the new limits are incompatible, that is, (high < low or low > high), then they will be rejected and the old limits retained. In addition, a counter limit error code will be returned. To avoid this situation when the limits are changed one at a time, a good rule to follow is: always move the high limit first when shifting the limits up and always move the low limit first when shifting them down.

As a 16-bit counter, the limit range is –32,768 to 32,767.

Count Mode

A counter can be configured to count continuously within the count limits, or to count to a limit and stop.

Continuous Counting

In the continuous counting mode, if either the upper or lower limit is exceeded, the counter wraps around to the other limit and continues counting. Continuous counting is the default mode.

Single-Shot Counting

If single-shot is selected, the counter will count to its upper or lower limit, then stop. When the counter is at the limit, the direction can be reversed and the counter will back away from the limit. The Accumulator can also be changed by loading a new value from the CPU or by applying a Preload Input.

Count Direction

Each of the four counters in the Type A configuration has only one Count Pulse input. The counter can be configured to increment or decrement its Accumulator on the rising edge of a Count Pulse input transition. The default is to count up.

Counter Timebase

For each counter, the Timebase represents a span of time which can be used to measure the rate of counting. For example, a program required to monitor the number of count pulses which occur every 30 seconds could use a Timebase of 30,000.

A timebase from 1 millisecond to 65535 milliseconds can be selected for each counter. The counter timebase is set to 1 second (1000 milliseconds) by default. The module stores the number of counts that occurred during the last-completed timebase interval in the Counts per Timebase register.

The timebase counter updates once each timebase period. After power-up, or any disruption in counting, allow at least one timebase period for the counter to stabilize.

Preload Value

For each counter, a starting, or Preload, value can be specified which will be used when the Preload input is activated. This Preload value is used for both hardware and software preloads. If the counter should be reset to zero, enter 0 as the Preload value; this is the default value. The Preload value range is –32,768 to +32,767, but it must be within the counter limits.

Strobe Mode

The Strobe Mode determines which Strobe input pulse the Strobe register will report. In Last mode, the Strobe register is always updated with the Accumulator value when the configured Strobe input transition occurs. Thus two rapid Strobe pulses could result in the first Strobe register value being missed. In First mode, the Strobe register is updated only if the Strobe flag set by a previous Strobe pulse has been acknowledged by setting the corresponding Reset Strobe %Q bit. In this mode, any subsequent Strobe pulses will be ignored and lost, but the first will always be retained. The default mode is Last.

Strobe Edge

Strobe inputs are edge sensitive. Each Strobe input on the module can be individually configured to have either the positive or the negative edge active. By default, they are positive-edge sensitive.

Strobe Effect

In the default mode, Strobe Only, a Strobe pulse only causes the Accumulator value to be copied into the Strobe register and the Strobe flag is set. In Strobe then Preload mode, a Strobe pulse will, in addition to copying the Accumulator into the Strobe Register, simultaneously perform a preload and set the Accumulator to the Preload value.

The Strobe then Preload mode should be used instead of tying the Strobe and Preload inputs together if every Strobe Pulse is to generate a Preload. When a Preload pulse occurs on the inputs at the same time as a Strobe pulse, or if the inputs are tied together, the Preload has precedence. The Accumulator will be set to the Preload value and then the Strobe register will be set to the Accumulator. Thus the Strobe register will obtain a copy of the Preload value.

Data Transfer Between High Speed Counter and CPU

The Series 90-70 High Speed Counter updates the %I and %AI data every 0.5 milliseconds. The Series 90-70 CPU reads this data immediately preceding every pass through the ladder logic, before triggering a ladder interrupt, and when a DOIO specifically requesting this data is performed in the ladder logic. To support the unique data coherency requirements of the High Speed Counter, the CPU reads both the %I and %AI data when performing DOIOs requesting only %I data.

The format of this input data depends on the counter configuration type. In return, during each I/O scan, the CPU sends 32 bits (%Q) of control data and 6 words (%AQ) of output data commands to the module. COMMREQ function blocks in the user program can also be used to send additional data commands to the module.

See Appendix A for more information about the COMMREQ and DOIO functions.

%I and %AI Data Sent by a Module Configured as Type A

The 32 status bits (%I) represent:

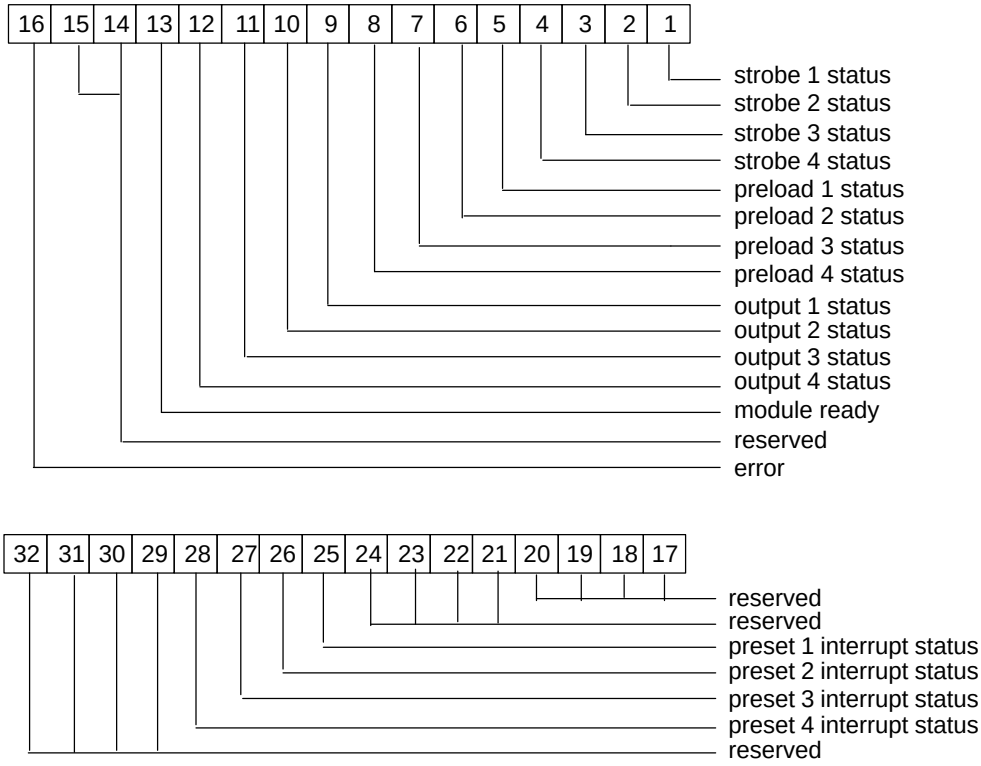
- Strobe status flag
- Preload status flag
- Preset Output status
- Module ready status
- Error status
- Interrupt status

These status bits are sent to the CPU as inputs, and can influence outputs sent from the CPU to the module.

The 16 register data words (%AI) represent:

- Module Status Codes
- Counts per Timebase value
- Accumulators
- Strobe Registers

Status Bits (%I)



Strobe Status

Each bit indicates when a Strobe Pulse occurs on the counter. If an application program uses this bit, it should be cleared by setting the corresponding Reset Strobe %Q bit. In First Strobe mode, additional strobes will be ignored until the Reset Strobe %Q bit is set.

Preload Status

Each bit indicates a rising edge of the Preload input on the counter. If an application program uses this bit, it should be cleared by setting the corresponding Reset Preload %Q bit.

Output Status

These bits indicate the ON or OFF state of the four preset outputs.

Module Ready

This bit is set after the module completes its power-up tests.

Error Status

This bit is set when an error occurs. If it is set, a module status code has been returned in the first %AI location and the board OK LED flashes at 4 Hz. The Error Status bit is cleared by setting the Clear Error %Q bit.

Preset Interrupt Status

These bits are set by the High Speed Counter when the corresponding preset output has changed state and generated an interrupt. These flags can be used by an interrupt routine to determine which outputs have generated interrupts. The Output Status bits can be used in conjunction with the Preset Interrupt Status bits to determine which transition caused the interrupt. The Preset Interrupt Status bits should only be tested in a ladder logic interrupt handler.

%AI Data

Word	Description	Word	Description
01	Module Status code	08	Accumulator for counter 2
02	Counts per timebase for counter 1	09	Strobe register for counter 2
03	Counts per timebase for counter 2	10	Accumulator for counter 3
04	Counts per timebase for counter 3	11	Strobe register for counter 3
05	Counts per timebase for counter 4	12	Accumulator for counter 4
06	Accumulator for counter 1	13	Strobe register for counter 4
07	Strobe register for counter 1	14 - 16	Not used (set to 0)

Module Status Codes

The Module Status Code in the %AI Input Data contains the error code returned to the PLC. The HSC sets this code to indicate a data command or configuration error. Once an error code has been returned, no more errors will be generated until the error is cleared. To clear a module status code, eliminate the condition that caused the error, and toggle the Clear Error %Q bit.

Note that fatal errors (RAM, EPROM) have no codes associated with them because these errors cause the watchdog timer to time out and the board to go into constant reset.

The error code format and a list of error codes are given below.

High Byte		Low Byte
Error Source	Counter or Preset #	Error Code

Error Codes for Type A

Error Code	Error Type	Definition
00	No Error	No Error Present
11	Command Errors	Unknown Command
21		Invalid Counter or Preset
31		Invalid COMMREQ Task ID
41		Velocity Increment Out of Range
81		Accumulator Out of Range
91		Preload Value Out of Range
C1		Preset ON Out of Range
D1		Preset Off Out of Range
12	Limit Errors	High Limit < Low Limit
22		Range Excludes Preload
52		Range Excludes Preset ON
62		Range Excludes Preset OFF
18	Configuration Errors	High Limit < Low Limit
28		Range Excludes Preload
58		Range Excludes Preset ON
68		Range Excludes Preset OFF
A8		Unsupported Feature Error
B8		Unknown Counter Type
C8		PLC Version Error
D8		Logicmaster 90 Version Error

Configuration Errors are not returned in %AI data since the module does not configure, but the error code is returned in the IO Fault data.

Counter or Preset Number

For a valid command (recognized value in byte 0), the counter or preset number, from 1 to 4, which generated the error will be reported in this nibble. A preset number only appears in error codes C1 and D1.

Error Source

Command and Limit errors return the source of the error.

Value	Error Source
1	%AQ Command 1 (%AQ Offset 0-2)
2	%AQ Command 2 (%AQ Offset 3-5)
4	COMMREQ Function

Example:

If the hexadecimal data 0002 0000 0107 (set Counter 1 Velocity Increment +131,072) was placed into the %AQ offsets 3 through 5, the error 2141h would be reported, since the maximum Velocity Increment is 100,000. The Module Status Code represents:

Value	Representation
2	Error in %AQ Command 2
1	Error generated by counter 1
41	Velocity Increment Out of Range

%Q and %AQ Data Sent from CPU to HSC Configured as Type A

Once each I/O scan, the CPU sends 8 words of data (32 bits of %Q and 6 words of %AQ) to the High Speed Counter Module. The application program can use these outputs to control the module.

The 32 output bits (%Q) represent:

- Reset Strobe flag
- Reset Preload flag
- Clear error flag
- Output enable
- Preload Accumulator

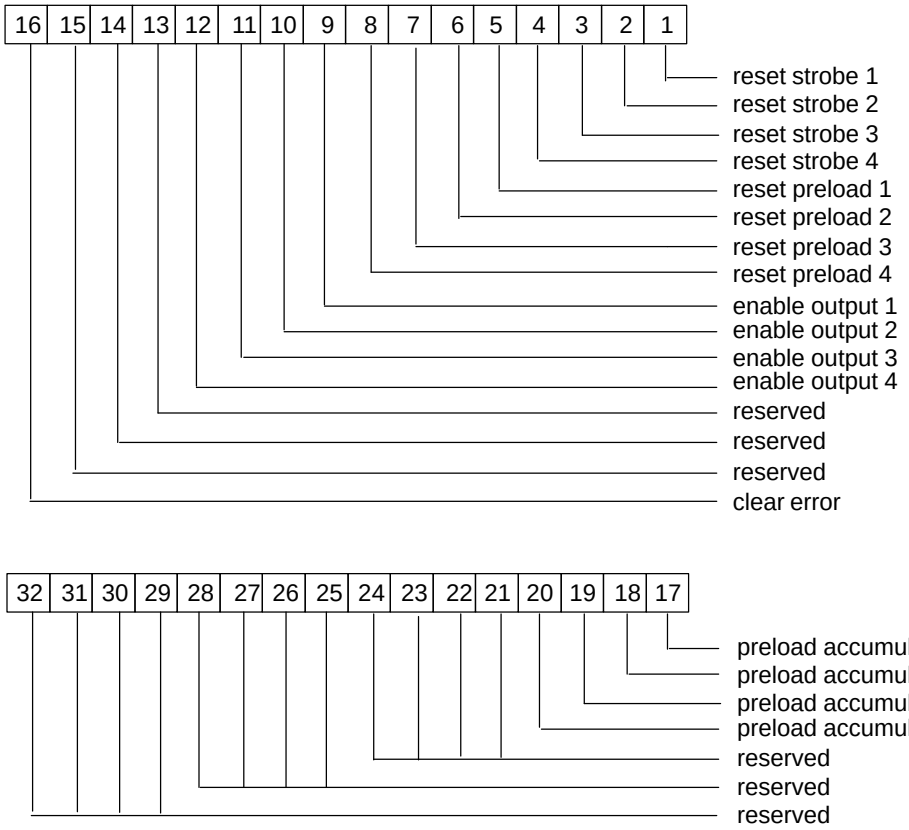
Six Words (%AQ) of Command Data

The 6 words of command data, which can also be sent using a COMMREQ Function Block, can perform the following operations:

- Load Accumulator
- Load count limits
- Load Accumulator increment
- Load output preset ON and OFF values
- Load Preload value
- Load time base
- Load Oscillator divider
- Set Count Direction
- Enable/Disableinterrupts

All of this data is transferred from the High Speed Counter to the CPU once per I/O scan. The I/O scan is active while the CPU is in the RUN mode or STOP ENABLED mode.

%Q Data



Reset Strobe

Setting this bit clears the corresponding Strobe Status %I bit. In First Strobe mode, subsequent strobe pulses are ignored until this bit is used to clear the Strobe Status bit.

Reset Preload

This bit is used to clear the corresponding Preload Status %I bit. For example, if a Preload occurred for counter 3, the Preload 3 Status %I bit would be set. To clear this bit so future Preloads can be detected, the Reset Preload 3 %Q bit must transition ON.

Enable Output

These bits enable the corresponding preset output. If cleared, the output will always be OFF and not reflect the accumulator's value in relation to the Preset ON and OFF values.

Clear Error

This bit should be set by the CPU to clear the Error Status %I bit after the error has been acknowledged. This bit is rising edge active, so new errors may appear while set.

Preload Accumulator

These bits tell the counter to perform a software preload and set the corresponding Accumulator to the Preload value. They do NOT, however, cause the corresponding Preload Status bit to be set.

Data Commands for Counter Type A

At the end of every CPU sweep, six words of %AQ data are automatically transferred from the CPU to the High Speed Counter. These six words are used to send data commands from the PLC to the HSC. The first three words, offsets 0 through 2, make up %AQ command 1, and the second three words, offsets 3 through 5, make up a completely separate %AQ command 2. Thus two commands can be sent to the HSC at the end of each sweep. Note that %AQ command 1 is executed first, so that if identical commands with different values are sent to the HSC simultaneously, %AQ command 2 data will overwrite %AQ command 1 data.

Even though the %AQ data is sent each sweep, commands are acted on ONLY if the command has changed since the last sweep. When any of the 6 bytes in a command changes, the HSC will accept the data as a new command and respond accordingly.

The DOIO function is supported, so that data can be transferred between the CPU and HSC mid-sweep. Note that to ensure that the High Speed Counter has time to process DOIO data sent to it, the application should not change the data more frequently than every 0.5 millisecond. Because data sent to the HSC is updated at the end of the CPU sweep, half a millisecond should elapse between the beginning of the sweep and a DOIO function block, between two DOIO function blocks, and between a DOIO function block and the end of the sweep.

The COMMREQ function block can also be used to send data commands to the HSC mid-sweep. COMMREQs must be separated only from each other, and by at least 0.5 milliseconds. A description and example of the use of COMMREQs and DOIOs is given in Appendix A.

%Q data is processed by the HSC before the %AQ data. Therefore commands that can be affected by %Q bit operations should be sent at least one sweep before the %Q bit operation. For example, the Load Preload Value command should be sent one sweep before setting the Preload Accumulator %Q bit to preload that value.

The High Speed Counter will check each command that is sent for validity. If the command syntax is incorrect, the counter will ignore the command and respond by flashing the Board Okay LED at 4 Hz, setting the Error Status %I bit, and returning a status code describing the error in the Module Status %AI word. The Error can be cleared by toggling the Clear Error %Q bit.

In describing data commands, word offsets are shown in reverse order and in hexadecimal to simplify data entry. The following example sends a Load Accumulator Counts command with value 0001 to counter 2 using offsets 0 through 2.

The first word, or command word, which goes into word offset 0 would be 0201h. The value 01 in byte 0 represents the command Load Accumulator Value. The value 02 in byte 1 is the counter number, in this case counter 2. For the Load Accumulator Value command, word 1 is the sixteen bit value to be loaded into the accumulator and word 2 is ignored.

In this example, word 1 would have the value 0001h because that is the value to be placed in the accumulator. Word 2 will be ignored and can be anything, but it is usually best to use the value 0. If word offset 0 corresponded to %AQ1, the complete command to load the counter 2 accumulator with value 0001 would be:

%AQ3 (word 2)	%AQ2 (word 1)	%AQ1 (word 0)
0000	0001	0201

The following table is a list of data commands for counter Type A.

Command Definition	Data				Command Word	
	Word 2		Word 1		Word 0	
	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
Null	xx	xx	xx	xx	xx	00h
Load Accumulator Value	xx	xx	data (16)		n	01h
Load High Limit	xx	xx	data (16)		n	02h
Load Low Limit	xx	xx	data (16)		n	03h
Load Accumulator Increment	xx	xx	xx	data (8)	n	04h
Set Counter Direction	xx	xx	xx	data (8)	n	05h
Load Timebase	xx	xx	data (16)		n	06h
Load Velocity	xx	data (24)			n	07h
Load Preset ON Value	xx	xx	data (16)		m	0Bh
Enable/Disable Preset ON Interrupt	xx	xx	xx	data (8)	m	0Fh
Load Preset OFF Value	xx	xx	data (16)		m	15h
Enable/Disable Preset OFF Interrupt	xx	xx	xx	data (8)	m	19h
Load Preload Value	xx	xx	data (16)		n	1Fh
Load Oscillator Divider	xx	xx	data (16)		0	32h

m = Preset Number (1 to 4); n = Counter Number (1 to 4);
xx = Do not care (ignored); data (8, 16, 24) = 8, 16, or 24 bit data

Descriptions of each command are given below. The valid range of values is given in parenthesis.

Null

This is the default %AQ data command. Since the %AQ data is transferred each PLC sweep, it is a good idea to have the Null command present when not executing a specific data command to avoid inadvertent execution. All data is ignored with a Null command.

Load AccumulatorValue (Low Limit to High Limit)

This command places a 16-bit value into a counter accumulator. The value must be within the Count Limits, or an error will be returned and the command ignored.

Load High Limit (–32768 to 32767)

This command sets the highest value to which a counter will count. Counts that would cause the counter to go higher are ignored or cause the accumulator to roll over to the Low Limit depending on whether the counter is configured for Single-shot or Continuous count mode. The High Limit can be any 16-bit value with the following restrictions: it must be greater than the Low Limit, the counter's Preload value must lie between it and the Low Limit, and all preset outputs which are assigned to the counter must have preset ON and OFF values which lie between it and the Low Limit.

If a restriction is not met, an error will be generated and the command ignored. If the range between the Low Limit and the new High Limit excludes the Accumulator, the Accumulator will be set to the Low Limit and no error is generated.

Load Low Limit (–32768 to 32767)

This command sets the lowest value to which a counter will count. Counts that would cause the counter to go lower are ignored or cause the accumulator to roll over to the High Limit depending on whether the counter is configured for Single-shot or Continuous count mode. The Low Limit can be any 16-bit value with the following restrictions: it must be less than the High Limit, the counter's Preload value must lie between it and the High Limit, and all preset outputs which are assigned to the counter must have preset ON and OFF values which lie between it and the High Limit.

If a restriction is not met, an error will be generated and the command ignored. If the range between the new Low Limit and the High Limit excludes the Accumulator, the Accumulator will be set to the Low Limit and no error is generated.

Load Accumulator Increment (–128 to 127 counts)

The Accumulator Increment performs a one-shot adjustment to the accumulator. Only byte 2 is used for data, all other data bytes are ignored. The one-shot increment may be performed at any time, even when counting at maximum rate. If the offset cause the counter to exceed its limits, the excess is treated just like any other overflow, i.e., in Continuous mode the Accumulator rolls over to the other limit and in Single-shot mode the Accumulator does not pass the limit.

Set Counter Direction (0=up, 1=down)

This command determines whether a counter's accumulator increments or decrements when there is a rising edge on its Count Pulse input. The direction may be set at any time.

Load Timebase (1 to 65535 milliseconds)

This command sets the timebase. The timebase is the number of milliseconds for which the counter counts input pulses and then returns in the Counts per Timebase register. If the timebase is 1000, or 1 second, the Counts per Timebase register returns the number of counts detected in each 1 second period. Any non-zero 16-bit value may be used as the timebase.

Load Velocity (–100,000 to 100,000 counts per second)

A velocity increment is an internal count generator, or a continuous accumulator increment. Each millisecond, 0.1% of the increment value is added to the accumulator. A value of 0 will stop the velocity increment. Counts from the velocity increment are cumulative with counts coming in from the Count Pulse input. Note that counts generated by the velocity increment are not reflected in the Counts per Timebase register.

Load ON and OFF Preset Value (Count Limits of the assigned counter)

This command sets the preset output turn on and turn off points within a counters range. Preset values can be any value between the high and low limits, inclusive.

Enable/Disable Preset ON and OFF Interrupts (0= Disable, 1= Enable)

This command enables or disables interrupts resulting from Preset output transitions. For example, if Preset ON interrupts are enabled, then a low to high transition of the

Preset ON output will generate an interrupt to the CPU. This command allows the interrupts to be enabled or disabled within a ladder.

Load Preload Value (Low Limit to High Limit)

The Load Preload command sets the value to which the Accumulator will be set when a positive edge occurs on the Preload input. The value must be between the High and Low Limits inclusive, or an error will be returned and the command ignored.

Load Oscillator Divider (1 to 65535)

This command changes the frequency of the square wave oscillator signal. The frequency generated is 1 megahertz (1 MHz) divided by the oscillator divider. Thus to get 50 Hz, the oscillator divider should be 20000.

Chapter 4 Counter Type B

Counter Type B is described in this chapter. The counter description includes counter operation, configuration of the counter, and the interface between the counter and the CPU.

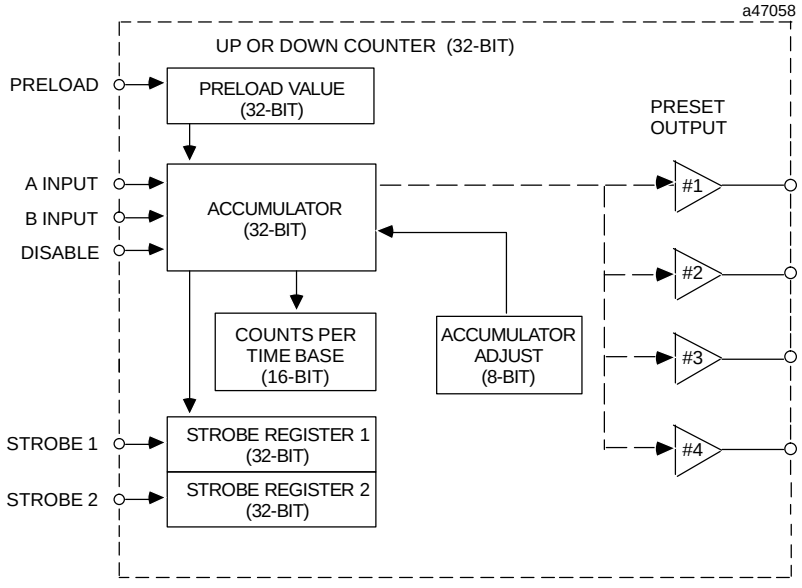
Contents and Operation of a Type B Counter

Overview

The Type B counter contains two 32-bit bidirectional counters. Each counter is controlled by 6 of the 12 single ended or differential voltage inputs: Count A, Count B, Strobe 1, Strobe 2, Disable, and Preload. Each counter may be independently configured to count in one of three modes: Up and Down, Pulse with Direction, and A Quad B. Counter Type B elements are shown in the figure below. Each counter has the following:

- a 32-bit Accumulator register which counts the pulses from the Count A and Count B inputs
- a Disable input which can make the Accumulator ignore the count pulses when asserted.
- two Strobe registers which store the Accumulator value when a Strobe input transitions
- a preload value which is inserted into the accumulator when a preload occurs
- a counts per timebase register which indicates the count rate of the input pulses.

Each of the four 5 to 30 V preset outputs can be independently assigned to either of the counters, and can be used to generate PLC interrupts.

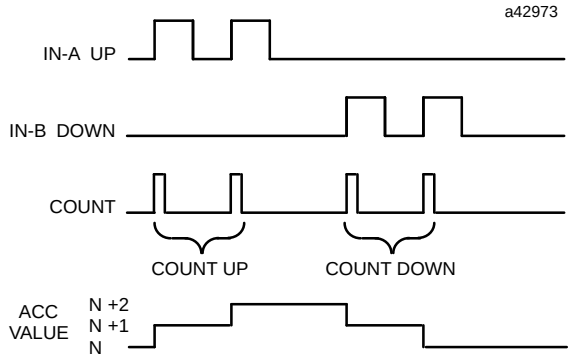


Count A and B Inputs and Accumulator

The 32-bit Accumulator is incremented or decremented based on a configured interpretation of its two count inputs. The interpretation can be set to Up / Down, Pulse / Direction, or A Quad B. Each is described below.

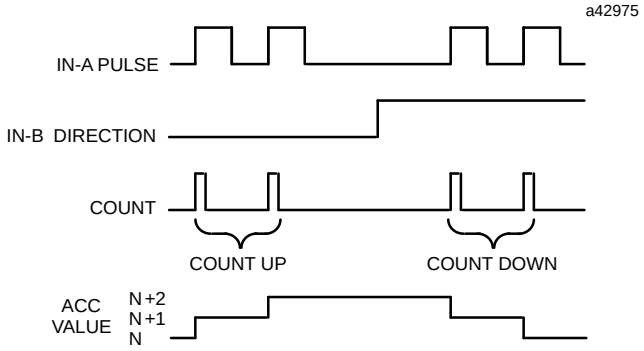
Operating in UP/DOWN Mode

Up-counting occurs on the low-to-high transition of the Up input. Down counting occurs on the low-to-high transition of the Down input. The accumulator automatically tracks the difference between the number of counts received by the Up channel and the Down channel. Simultaneous inputs on the up channel and down channel will cause a net accumulator change of zero.



Operating in Pulse/Direction Mode

Counting always occurs on the low-to-high transition of the Pulse input. Count direction is up for a low level on the Direction input and down for a high level on the Direction input. Avoid changing the Direction signal coincidentally with the rising edge of the Pulse input.

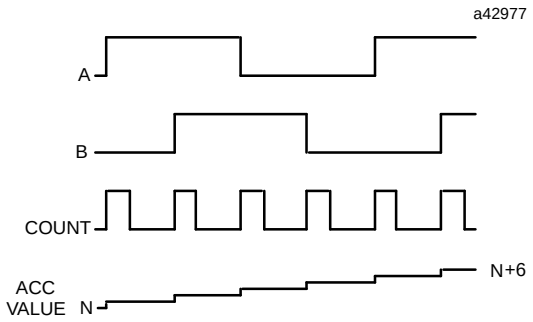


Operating in A Quad B Mode

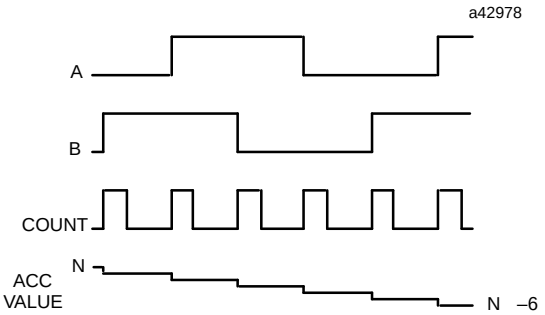
In A Quad B mode, there are four counts for each A Quad B cycle. A count occurs for each transition of either A or B. The counts will be evenly spaced with respect to the input waveforms when the phase relationship between A and B is shifted by 1 / 4 cycle.

The phase relationship between A and B determines count direction, as shown in the following timing diagrams.

The count direction is up if A leads B.



The count direction is down if A lags B.



The Accumulator is bounded by configurable High and Low Limits. The interaction between the Accumulator and the limits depends on the configured count mode. In Continuous mode, the Accumulator will increment or decrement to the current High or Low Limit, roll over to the other limit, and continue counting. In Single Shot mode, the Accumulator will count to the current High or Low Limit and stop. If the counter direction is changed, the Accumulator will count away from the limit until it reaches the other limit.

The High and Low Limits can be changed to any valid 32-bit value at any time using a data command from the PLC. To be a valid 32-bit value, the following conditions must be met:

- the High Limit must be greater than the Low Limit
- the Preload value must be within the High and Low Limit bounds
- any presets assigned to the counter must have ON and OFF values within the High and Low Limit bounds.

If the limits are changed so the Accumulator is outside the limit boundaries, the Accumulator is set to the Low Limit.

The Accumulator may be set to any 32-bit value within the bounds of the High and Low limits at any time using a data command. Another data command allows the Accumulator to be adjusted by a byte increment value, from –128 to +127 counts. Finally, a velocity can be commanded which causes the Accumulator to increment or decrement at a fixed rate.

Strobe Inputs and Register

Each Strobe input is an edge sensitive input which can be configured to respond to either a positive edge or a negative edge. When the configured Strobe input transition occurs (referred to as a Strobe Pulse) the value in the Accumulator is stored in the corresponding Strobe register and a strobe flag is set and returned in %I data to indicate the event to the CPU. The application program in the CPU acknowledges receipt of the strobe by toggling the corresponding Strobe Status %Q bit.

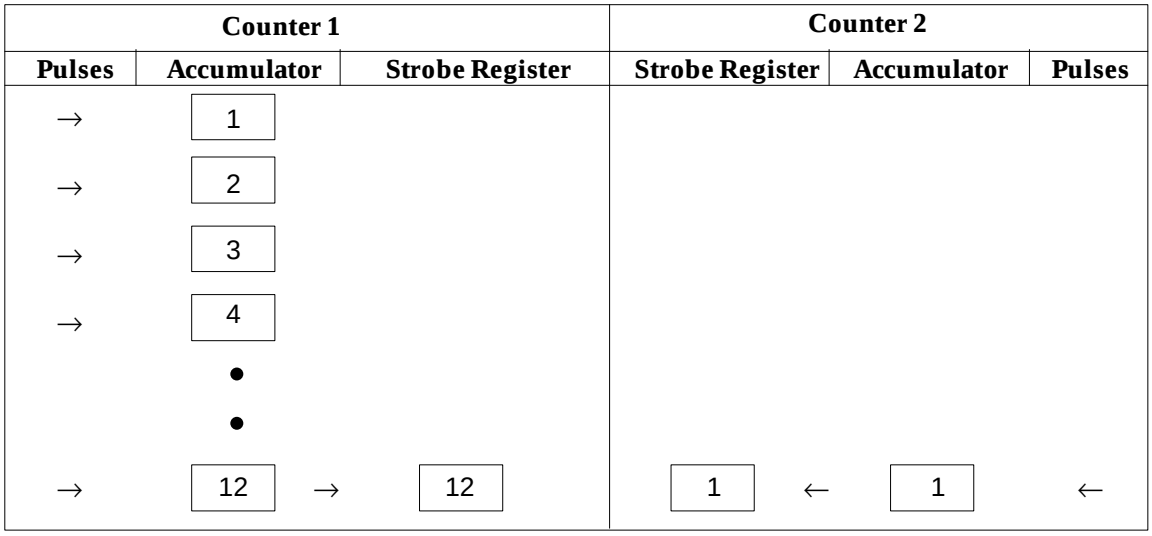
Two strobe modes are available to select which Strobe value is most important. **In Last Strobe mode, the default, a Strobe Pulse will always update the Strobe register with the latest Accumulator value regardless of the Strobe Status flag.** In First Strobe mode, the first Strobe is captured and all subsequent Strobe input transitions are ignored until the strobe flag is cleared by toggling the corresponding Reset Strobe %Q bits.

Strobe Linkage

Normal strobe operation is achieved by setting the Strobe Linkage parameter to Independent. In Independent Mode, Strobes 1.1 and 1.2 strobe the Accumulator 1 value when a Strobe Pulse occurs, and Strobes 2.1 and 2.2 strobe the Accumulator 2 value when a Strobe Pulse occurs. Counter Type B has the capability of linking Strobes 1.1 and 2.1 to a change in Accumulator 2 instead of their respective Strobe pulses. In Coupled to Accumulator 2 mode, any count pulses which change Accumulator 2 will cause Strobe 1.1 to strobe the Accumulator 1 value and Strobe 2.1 to strobe the Accumulator 2 value. Pulses on Strobes 1.1 and 2.1 while in this mode are ignored. Strobes 1.2 and 2.2 operate normally.

This feature can be used to accurately measure a pulse rate against a reference pulse, or to compare two different pulse rates. The reference pulse is connected to Counter 1 inputs and the slower pulse that is to be measured is connected to Counter 2 inputs.

The following illustration represents two pulses. Counter 1 pulses twelve times faster than Counter 2. Each time Counter 2 pulses, its Strobe Register 1 and Counter 1's Strobe Register 1 are loaded with their Accumulator values.



Input terminal connections for Strobe Input 1 for Counter 1 and Strobe input 1 for Counter 2 are not used with this feature.

Preload Input and Value

The Preload input is normally used to perform a reset function for the counter. The value to which the Accumulator is set when a preload occurs can be configured to any 32-bit value within the range of the high and low limits and has a default value of zero. The Preload value can also be changed using a data command from the PLC. There are two types of Preloads, hardware and software.

A hardware preload uses the the Preload input and is positive edge sensitive only. On the positive transition, the configured preload value is inserted into the accumulator and a preload flag is set and returned in %I data to indicate the event to the CPU. If an application program uses this flag indication, it can use the corresponding %Q bit to clear the preload flag before the next preload occurs. **A rising edge on the Preload input always preloads the Accumulator regardless of the state of the Preload flag.**

Note that when a pulse occurs on the Preload inputs at the same time as a Strobe pulse, or if the inputs are tied together, the Preload has precedence. The Accumulator will be set to the Preload value and then the Strobe register will be set to the Accumulator. This means that he Strobe register will have a copy of the Preload value.

A software preload can be performed by setting a Preload Accumulator %Q bit. On the positive transition of this %Q bit, the current preload value is placed into the Accumulator. A software preload does NOT set the Preload flag.

Counts per Timebase Register

The Counts per Timebase register is a 16-bit register which contains the number of counts received on the Count Pulse input in the last completed timebase interval. It is used to measure the rate of counting. If more counts are received than can be stored in a 16-bit register, the register will overflow. The timebase interval is a configurable value from 1 to 65535 milliseconds.

Changes to the timebase will not take effect until after the previous timebase and one new timebase have elapsed. A Preload will interrupt counting and cause the Counts per Timebase register to be inaccurate for up to two timebase intervals. The timebase is initially configured as 1 second, but may be changed using the Logicmaster 90-70 Configurator function or a data command.

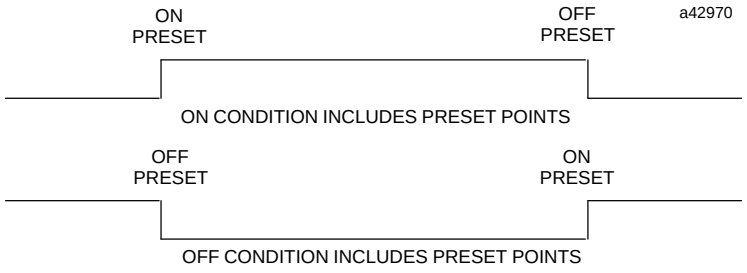
As an unsigned number, the Counts per Timebase register will correctly indicate from 0 to 65536 positive counts received per timebase. As a signed number, it will properly indicate from –32768 to 32767 counts per timebase. The timebase should be selected to not allow more counts in a timebase than the 16-bit register can hold or it will overflow.

Preset Outputs

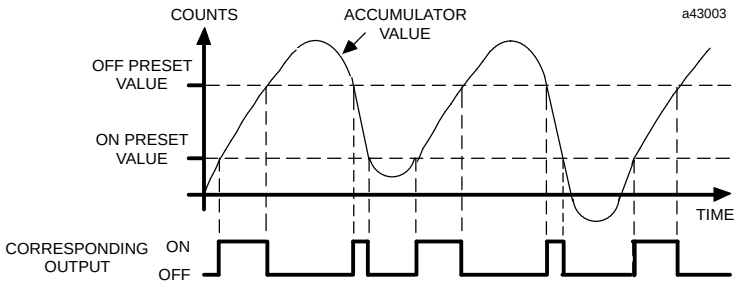
The module has four preset outputs, each of which can be assigned to any counter. Each preset output has a preset ON and preset OFF value, or position, which must be within the count limits of the counter to which the preset is assigned. The preset ON and OFF positions determine when the output will be ON or OFF as shown below.

Preset closest to low limit	Output ON	Output OFF
ON	> = ON Preset < = OFF Preset	> OFF Preset < ON Preset
OFF	< OFF Preset > ON Preset	< = ON Preset > = OFF Preset

The output may be either on or off when the accumulator value lies between the Preset points.



For example:



Separation of Preset Points

The count accumulators are compared to the Presets at 0.5 msec intervals. Therefore, to guarantee that the outputs will always switch, the Preset points must be separated by at least the number of counts received in a 0.5 msec time period. For example:

If maximum count rate = 10kHz;
then minimum count separation = (10,000 Hz x .0005 sec) = 5 counts.

Preset Interrupts

Interrupts can be enabled or disabled for each preset output's ON and OFF transition. At the same time a preset output changes state, the CPU is interrupted. %I and %AI data is transferred so that the interrupt routine will see the most current data from the High Speed Counter. Simultaneous preset changes generate only one interrupt to the CPU, so the updated %I data must be used by an interrupt routine to determine which presets changed state and which edge(s) generated the interrupt. Once configured, interrupts can be independently enabled or disabled using data commands. See Appendix B for information on using the interrupt capability.

Output Failure Mode

When the CPU is stopped or lost, counter operation continues normally without interfacing to the CPU. Preset output operation during this stopped state can be configured for one of three modes. In Normal mode, the outputs continue to operate as if the CPU were present. Outputs will change state to reflect the counter Accumulators. In Force Off mode, all preset outputs are turned off and remain off until the CPU returns. In Holdlast mode, the preset outputs retain current levels and do not reflect the counter Accumulators. If the CPU returns to operation, the outputs will immediately begin reflecting the counter Accumulators.

Oscillator Output

The High Speed Counter module generates a 5V square wave oscillator signal. The oscillator output frequency is determined by the current oscillator divider (set in configuration or by data command) as indicated below:

Oscillator Frequency (Hz) = 1,000,000 / oscillator divider

The output frequency ranges from approximately 15 Hz (oscillator divider of 65535) to 1 MHz (oscillator divider of 1).

Table 4-1. Type B Specific Terminal Strip Assignments

Pin	Signal Name	Type B Pin Name	Type B Pin Description
1,3	IN1	COUNTINPUT1A	Counter 1 count A input
2,4	IN2	COUNTINPUT1B	Counter 1 count B input
5,7	IN3	COUNTINPUT2A	Counter 2 count A input
6,8	IN4	COUNTINPUT2B	Counter 2 count B input
11,13	IN5	PRELOAD1	Counter 1 preload input
12,14	IN6	DISABLE1	Counter 1 disable input
15,17	IN7	PRELOAD2	Counter 2 preload input
16,18	IN8	DISABLE2	Counter 2 disable input
21,23	IN9	STROBE 1.1	Counter 1 strobe 1 input
22,24	IN10	STROBE 1.2	Counter 1 strobe 2 input
25,27	IN11	STROBE 2.1	Counter 2 strobe 1 input
26,28	IN12	STROBE 2.2	Counter 2 strobe 2 input

Configuring the Type B High Speed Counter

The following table summarizes all configuration features and default configuration values for the Type B counter.

Configuration Parameter	Description	Values	Default
Failure Mde	Output Failure Mode	NORMAL, OFF, HOLD	NORMAL
Osc Divider	Oscillator Divider	1 ... 65535	1000
Count Thrshlds	Count Input Thresholds	NON-TTL, TTL, MAG-PKUP	NON-TTL
Control Thrshlds	Control Input Thresholds	NON-TTL, TTL	NON-TTL
Count Filtr	Count Input Filter	HIFREQ, LOWFREQ	HIFREQ
Preld Filtr	Preload Input Filter	HIFREQ, LOWFREQ	HIFREQ
Disbl Filtr	Disable Input Filter	HIFREQ, LOWFREQ	HIFREQ
Preset CTR#	Preset Accumulator	CTR1 ... CTR4	Preset #
On	Preset ON setpoint	Low Limit ... High Limit	8,388,607
Off	Preset OFF setpoint	Low Limit ... High Limit	0
ON Interrupt	Preset on transition interrupt	DISABLED, ENABLED	DISABLED
OFF Interrupt	Preset off transition interrupt	DISABLED, ENABLED	DISABLED
Hi Limit	High Count Limit	–2,147,483,648 ... 2,147,483,647	8,388,607
Lo Limit	Low Count Limit	–2,147,483,648 ... 2,147,483,647	0
Count Mode	Count Mode	CONTINU, SINGSHOT	CONTINU
Count Sig	Count Signals	PULSE / DIR, UP, DOWN, A QUAD B	PULSE / DIR
Timebase(ms)	Timebase	1 ... 65535 ms	1000 ms
Preld Value	Preload Value	Low Limit ... High Limit	0
Strobe Mode	Strobe Mode	LAST, FIRST	LAST
Strobe 1 Edge	Strobe 1 Edge	POS, NEG	POS
Strobe 2 Edge	Strobe 2 Edge	POS, NEG	POS
Strb Lnk	Strobe Linkage	IND, ACC2	IND

Output Failure Mode

When the CPU is stopped or lost, counter operation continues normally; however, the operation of the Preset outputs can be configured until the CPU returns or power is cycled. In all modes, the Accumulators are updated and the Strobes and Preloads are processed normally.

- In Normal mode (NORMAL), the outputs continue to operate as if the CPU were present. Outputs will change state to reflect the counter Accumulators.
- In Force Off mode (OFF), all preset outputs are turned off and remain off until the CPU returns.
- In Holdlast mode (HOLD), the preset outputs retain current levels and do not reflect the counter Accumulators.

If the CPU returns to operation or the module is power-cycled, the outputs will immediately begin reflecting the counter Accumulators again.

Oscillator Divider

The oscillator divider is used to generate a 5V oscillator output. The output frequency is 1 million divided by the oscillator divider; the formula is shown below.

Oscillator Frequency (Hz) = 1,000,000 / oscillator divider

The output frequency ranges from approximately 15 Hz (oscillator divider of 65535) to 1 MHz (oscillator divider of 1).

Input Thresholds

All inputs can be used as differential or single-ended inputs. The following table specifies the input thresholds for single-ended and differential use based on threshold selection and input type. The configuration parameters will set input thresholds according to the following table:

Configuration Parameter	Inputs Controlled	Input Definitions
Counter 1 Threshold	IN1, IN2	Counter 1, Inputs A, B
Counter 2 Threshold	IN3, IN4	Counter 2, Inputs A, B
Control 1 Threshold	IN5, IN6, IN9, IN10	Preload, Disable, Strobe 1.1, 1.2
Control 2 Threshold	IN7, IN8, IN11, IN12	Preload, Disable, Strobe 2.1, 2.2

Note that all the inputs controlled will have the same voltage threshold.

The voltage thresholds which can be selected for each input are described in the following table.

Input Type	Single-Ended			Differential		
	Non-TTL	TTL	Mag-Pickup	Non-TTL	TTL	Mag-Pickup
Counter 1 Threshold	8 V	1.4 V	0.1 V	4.8 V	0.8 V	0.1 V
Counter 2 Threshold	8 V	1.4 V	0.1V	4.8 V	0.8 V	0.1V
Control 1 Threshold	8 V	1.4 V	X	4.8 V	0.8 V	X
Control 2 Threshold	8 V	1.4 V	X	4.8 V	0.8 V	X

Input Filters

All inputs default to using a 2.5 microsecond high-frequency filter. Each Count, Preload, and Disable input can be configured to use a 12.5 millisecond low-frequency filter instead. The low-frequency filter reduces the effects of signal noise. The Strobe inputs always use the high-frequency filter.

Preset Accumulator

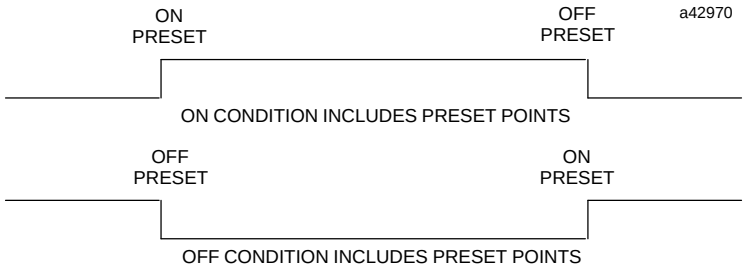
The Preset Accumulator field determines which counter a preset output will reflect. Each of the four preset outputs can be assigned to any of the accumulators. The Preset ON and Preset OFF values must be within the range of the High and Low Limits of the counter the Preset Accumulator is assigned to. The default configuration sets Presets 1 and 2 to counter 1, and Presets 3 and 4 to counter 2.

Output Preset ON and OFF Positions

Each preset output has a preset ON and OFF position. The output state reflects the counter accumulator value in relation to the ON and OFF points.

Preset closest to low limit	Output ON	Output OFF
ON	> = ON Preset < = OFF Preset	> OFF Preset < ON Preset
OFF	< OFF Preset > ON Preset	< = ON Preset > = OFF Preset

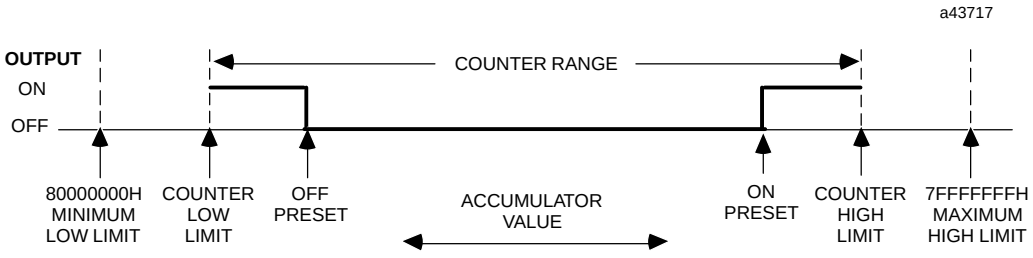
The output may be either on or off when the accumulator value lies between the Preset points.



Location of Preset Points

The Preset points may be located anywhere within the counter range. When the accumulator value is between the Preset points, the output ON / OFF state will always be that of the lowest (most negative) Preset point. When the accumulator value is *not* between the Preset points, the output ON / OFF state will be that of the most positive preset. This is true regardless of the counter direction.

The following diagram illustrates the Preset Output state when the OFF Preset is closer to the low limit than the ON Preset.



Preset Interrupt Enables

Each preset can generate an interrupt to the CPU. If the Interrupt ON selection is enabled, then an ON transition of the preset output will generate an interrupt to the CPU. Similarly, if the Interrupt OFF selection is enabled, an OFF transition of the preset output will generate an interrupt to the CPU. Thus no edge, either edge, or both edges of a preset output transition can generate an interrupt. The default is for all interrupts to be disabled.

Count Limits

Each counter is assigned upper and lower count limits. The upper (high) limit must the most positive, and the lower limit must be the most negative. Both limits can be positive or negative, but the high limit must always be greater than the low limit. A counter's Accumulator, Preload value, and any Preset outputs assigned to the counter must lie within the high and low limits.

If the Accumulator value is outside the new limits when the limits are changed it is automatically adjusted to the low limit value. If the new limits are incompatible, that is, (high < low or low > high), then they will be rejected and the old limits retained. In this case a counter limit error code will be returned. To avoid this situation when the limits are changed one at a time, a good rule to follow is: always move the high limit first when shifting the limits up and always move the low limit first when shifting them down.

As a 32-bit counter, the limit range is –2,147,483,648 to 2,147,483,647.

Count Mode

A counter can be configured to count continuously within the count limits, or to count to a limit and stop.

Continuous Counting

In the continuous counting mode, if either the upper or lower limit is exceeded, the counter wraps around to the other limit and continues counting. Continuous counting is the default mode.

Single-Shot Counting

If single-shot is selected, the counter will count to its upper or lower limit, then stop. When the counter is at the limit, counts in the opposite direction will count it back off the limit. The Accumulator can also be changed by loading a new value from the CPU or by applying a Preset Input.

Count Signal Mode

Each counter can be configured to interpret its Count inputs in one of three ways:

- Up / Down mode - rising edges on the A, or up, input increment the Accumulator while positive transitions on the B, or down, input decrement the Accumulator.
- Pulse / Direction mode - rising edges on the A, or pulse, input are counted. If the B, or direction, input is low then the Accumulator is incremented but if the Second input is high then the Accumulator is decremented.
- A Quad B mode - if the A input leads the B input, the Accumulator is incremented and if the B input leads the A input the Accumulator is decremented.

Counter Timebase

For each counter, the Timebase represents a span of time which can be used to measure the rate of counting. For example, a program required to monitor the number of count pulses that occur every 30 seconds could use a Timebase of 30,000.

A Timebase from 1 millisecond to 65535 milliseconds can be selected for each counter. The counter timebase is set to 1 second (1000 milliseconds) by default. The module stores the number of counts that occurred during the last-completed timebase interval in theCounts / Timebase register. The timebase value selected should not allow the Counts / Timebase register to overflow at the maximum count frequency.

The timebase counter updates once each timebase period. After power-up, or any disruption in counting, allow at least one timebase period for the counter to stabilize.

Preload Value

For each counter, a starting, or Preload, value can be specified which will be used when the Preload input is activated. This Preload value is used for both hardware and software preloads. If the counter should be reset to zero, enter 0 as the Preload value; this is the default value. The preload range is –2,147,483,648 to +2,147,483,647.

Strobe Mode

The Strobe Mode determines which Strobe input pulse the Strobe register will report. In Last mode, the Strobe register is always updated with the Accumulator value when the configured Strobe input transition occurs. Therefore, two rapid Strobe pulses could result in the first Strobe register value being missed. In First mode, the Strobe register is updated only if the Strobe flag set by a previous Strobe pulse has been acknowledged by setting the corresponding reset Strobe %Q bit. In this mode, any subsequent Strobe pulses will be ignored and lost, but the first will always be retained. The default mode is Last.

Strobe Edge

Strobe inputs are edge sensitive. Each Strobe input on the module can be individually configured to have either the positive or the negative edge active. By default, they are positive-edge sensitive.

Strobe Linkage

The Strobe Linkage selects whether strobes for each counter operate independently or are linked to Accumulator 2. In Independent mode, Strobe Pulses strobe their respective Accumulators. In Accumulator 2 mode, normal Strobe 1.1 and 2.1 operations are disabled. Strobe 1.1 and 1.2 are triggered whenever the Counter 2 Accumulator changes.

Data Transfer Between High Speed Counter and CPU

The Series 90-70 High Speed Counter updates the %I and %AI data every 0.5 milliseconds. The Series 90-70 CPU reads this data immediately preceding every pass through the ladder logic, before triggering a ladder interrupt, and when a DOIO specifically requesting this data is performed in the ladder logic. To support the unique data coherency requirements of the High Speed Counter, the CPU reads both the %I and %AI data when performing DOIOs requesting only %I data.

The format of this input data depends on the counter configuration type. In return, during each I/O scan, the CPU sends 32 bits (%Q) of control data and 6 words (%AQ) of output data commands to the module. COMMREQ function blocks in the user program can be used to send additional data commands to the module.

See Appendix A for more information about the COMMREQ and DOIO functions.

%I and %AI Data Sent by a Module Configured as Type B

The 32 status bits (%I) represent:

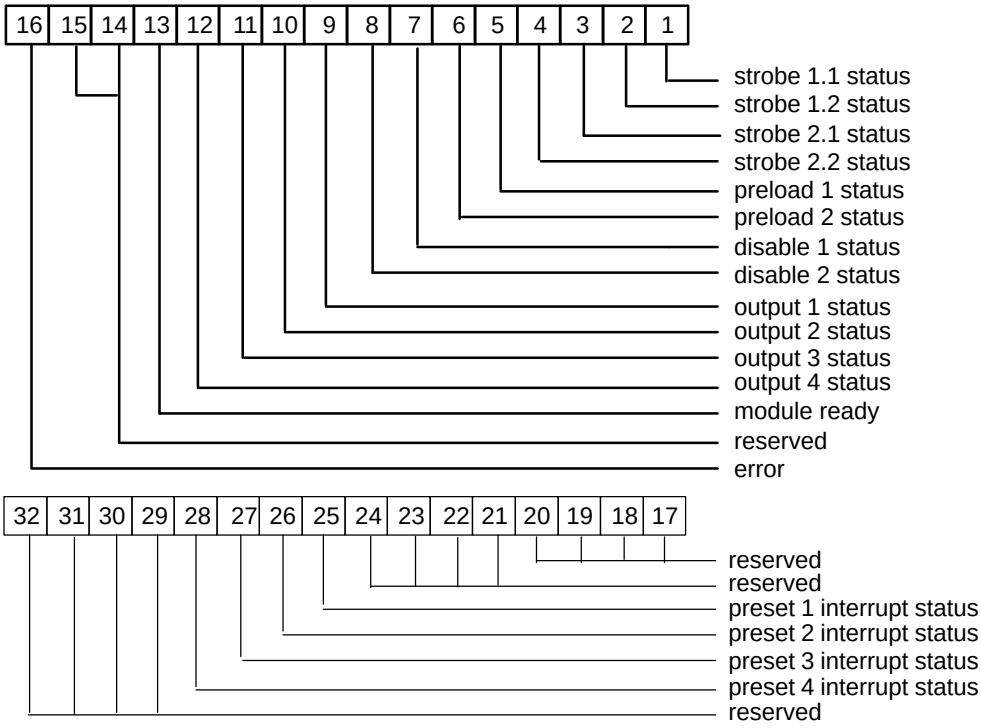
- Strobe status flag
- Preload status flag
- Disable status
- Preset Output status
- Module ready status
- Error status
- Interrupt status

These status bits are sent to the CPU as inputs, and can influence outputs sent from the CPU to the module.

The 16 register data words (%AI) represent:

- Counts per Timebase value
- Accumulators
- Strobe Registers
- module status code

Status Bits (%I) - Type B Counter



Strobe Status

Each bit indicates when a Strobe Pulse occurs on the counter. If an application program uses this bit, it should be cleared by setting the corresponding Reset Strobe %Q bit. In First Strobe mode, additional strobes will be ignored until the Reset Strobe %Q bit is set.

Preload Status

Each bit indicate a rising edge of the corresponding Preload input on the counter. If an application program uses these bits, it should clear them by setting the corresponding Reset Preload %Q bit.

Disable Status

These bits indicate the level of the Disable inputs and whether counting is disabled. When set, the Disable input is ON and count inputs are ignored.

Output Status

These bits indicate the ON or OFF state of the four preset outputs.

Module Ready

This bit is set after the module completes its power-up tests.

Error Status

This bit is set when an error occurs. If it is set, a module status code has been returned in the first %AI location and the board OK LED flashes at 4 Hz. The Error Status bit is cleared by setting the Clear Error %Q bit.

Preset Interrupt Status

These bits are set by the High Speed Counter when the corresponding preset output has changed state and generated an interrupt. These flags can be used by an interrupt routine to determine which outputs have generated interrupts. The Output Status bits can be used in conjunction with the Preset Interrupt Status bits to determine which transition caused the interrupt. The Preset Interrupt Status bits should only be tested in a ladder logic interrupt handler.

%AI Data - Type B Counter

Word	Description
01	Module Status code
02	Counts per timebase for counter 1
03	Counts per timebase for counter 2
04-05	Accumulator for counter 1
06-07	Strobe register 1 for counter 1
08-09	Strobe register 2 for counter 1
10-11	Accumulator for counter 2
12-13	Strobe register 1 for counter 2
14-15	Strobe register 2 for counter 2
16	Unused

Module Status Codes

The Module Status Code in the %AI Input Data contains the error code returned to the PLC. The HSC sets this code to indicate a data command or configuration error. Once an error code has been returned, no more errors will be generated until the error is cleared. To clear a module status code, eliminate the condition that caused the error, and toggle the Clear Error %Q bit.

Note that fatal errors (RAM, EPROM) have no codes associated with them because these errors cause the watchdog timer to time out and the board to go into constant reset.

The error code format and a list of error codes are given below.

High Byte		Low Byte
Error Source	Counter or Preset #	Error Code

Error Codes for Type B Counter

Error Code	Error Type	Definition
00	No Error	No Error Present
11	Command Errors	Unknown Command
21		Invalid Counter or Preset
31		Invalid COMMREQ Task ID
41		Velocity Increment Out of Range
81		Accumulator Out of Range
91		Preload Value Out of Range
C1		Preset ON Out of Range
D1		Preset Off Out of Range
12	Limit Errors	High Limit < Low Limit
22		Range Excludes Preload
52		Range Excludes Preset ON
62		Range Excludes Preset OFF
18	Configuration Errors	High Limit < Low Limit
28		Range Excludes Preload
58		Range Excludes Preset ON
68		Range Excludes Preset OFF
A8		Unsupported Feature Error
B8		Unknown Counter Type
C8		PLC Version Error
D8		Logicmaster 90 Version Error

Configuration Errors are not returned in %AI data since the module does not configure, but the error code is returned in the IO Fault Table additional fault information, which is accessed by pressing **Ctrl-F**.

Counter or Preset Number

For a valid command (recognized value in byte 0), the counter (1 or 2) or preset number, 1 to 4, which generated the error will be reported in this nibble. A preset number only appears in error codes C1 and D1.

Error Source

Command and Limit errors return the source of the error.

Value	Error Source
1	%AQ Command 1 (%AQ Offset 0-2)
2	%AQ Command 2 (%AQ Offset 3-5)
4	COMMREQ Function

Example:

If the hexadecimal data 0002 0000 0107 was placed into the %AQ offsets 3 through 5, the error 2141h would be reported. The Module Status Code represents:

Value	Representation
2	Error in %AQ Command 2
1	Error generated by counter 1
41	Velocity Increment Out of Range

%Q and %AQ Data Sent from CPU to HSC Configured as Type B

Once each I/O scan, the CPU sends eight words of data (32 bits of %Q and six words of %AQ) to the High Speed Counter Module. The application program can use these outputs to send commands to the module.

The 32 output bits (%Q) represent:

- Reset Strobe flag
- Reset Preload flag
- Clear error flag
- Output enable
- Accumulator preload

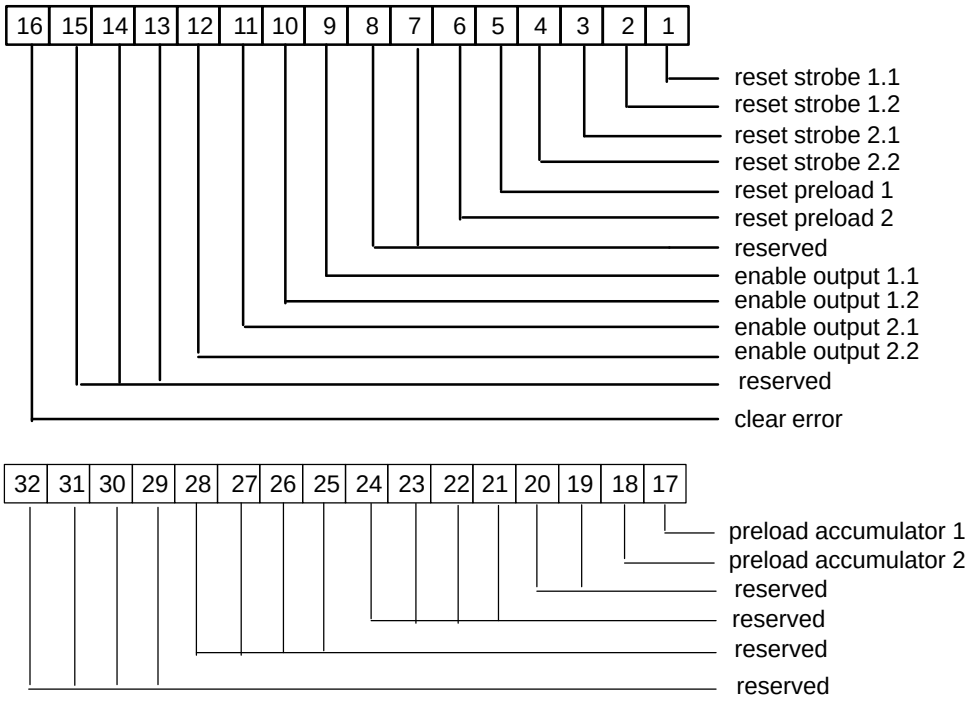
Six words (%AQ) of Command Data

The 6 words of command data, which can also be sent using a COMMREQ Function Block, can perform the following operations:

- Load Accumulator
- Load count limits
- Load Accumulator increment
- Load output preset on and off values
- Load Preload values
- Load time base
- Load Oscillator divider
- Enable/Disable interrupts

All of this data is transferred from the High Speed Counter to the CPU once per I/O scan. The I/O scan is active while the CPU is in the RUN mode or STOP ENABLED mode.

%Q Data - Type B Counter



Reset Strobe

Setting this bit clears the corresponding Strobe Status %I bit. In First Strobe mode, subsequent strobe pulses are ignored until this bit is used to clear the Strobe Status bit.

Reset Preload

This bit is used to clear the corresponding Preload Status %I bit. For example, if a Preload occurred, the Preload Status %I bit would be set. To clear this bit so future Preloads can be detected, the Reset Preload %Q bit must transition ON.

Enable Output

These bits enable the corresponding preset output. If cleared, the output will always be OFF and not reflect the accumulator's value in relation to the Preset ON and OFF values.

Clear Error

This bit should be set by the CPU to clear the Error Status %I bit after the error has been acknowledged. This bit is rising edge active, so new errors may appear while set.

Preload Accumulator

These bits tell the counter to perform a software preload and set the corresponding Accumulator to the Preload value. They do NOT, however, cause the corresponding Preload Status bit to be set.

Data Commands for Counter Type B

At the end of every CPU sweep, six words of %AQ data are automatically transferred from the CPU to the High Speed Counter. These six words are used to send data commands from the PLC to the HSC. The first three words, offsets 0 through 2, make up %AQ command 1, and the second three words, offsets 3 through 5, make up a completely separate %AQ command 2. Thus two commands can be sent to the HSC at the end of each sweep. Note that %AQ command 1 is executed first, so that if identical commands with different values are sent to the HSC simultaneously, %AQ command 2 data will overwrite %AQ command 1 data.

Even though the %AQ data is sent each sweep, commands are acted on ONLY if the command has changed since the last sweep. When any of the 6 bytes in a command changes, the HSC will accept the data as a new command and respond accordingly.

The DOIO function is supported, so that data can be transferred between the CPU and HSC mid-sweep. Note that to ensure that the High Speed Counter has time to process DOIO data sent to it, the application should not change the data more frequently than every 0.5 millisecond. Because data sent to the HSC is updated at the end of the CPU sweep, half a millisecond should elapse between the beginning of the sweep and a DOIO function block, between two DOIO function blocks, and between a DOIO function block and the end of the sweep.

The COMMREQ function block can also be used to send data commands to the HSC mid-sweep. COMMREQs must be separated only from each other, and by at least 0.5 milliseconds. A description and example of the use of COMMREQs and DOIOs is given in Appendix A.

%Q data is processed by the HSC before the %AQ data. Therefore commands that can be affected by %Q bit operations should be sent at least one sweep before the %Q bit operation. For example, the Load Preload Value command should be sent one sweep before setting the Preload Accumulator %Q bit to preload that value.

In describing data commands, word offsets are shown in reverse order and in hexadecimal to simplify data entry. The following example sends a Load Accumulator Counts command with value 0001 to counter 2 using offsets 0 through 2.

The first word, or command word, which goes into word offset 0 is 0201h. The value 01 in byte 0 represents the command Load Accumulator Value. The value 02 in byte 1 is the counter number, in this case counter 2. For the Load Accumulator Value command, word 1 is the 16-bit value to be loaded into the accumulator and word 2 is ignored. In this example, word 1 would have the value 0001h because that is the value to be placed in the accumulator. Word 2 will be ignored and can be anything, but it is usually best to use the value 0. If word offset 0 corresponded to %AQ1, the complete command to load the counter 2 accumulator with value 0001 would be:

%AQ3 (word 2)	%AQ2 (word 1)	%AQ1 (word 0)
0000	0001	0201

The following table is a list of data commands for counter Type B. Byte 0 data is in hexadecimal.

Command Definition	Data				Command Word	
	Word 2		Word 1		Word 0	
	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
Null	xx	xx	xx	xx	xx	00h
Load Accumulator Value	data (32)				n	01h
Load High Limit	data (32)				n	02h
Load Low Limit	data (32)				n	03h
Load Accumulator Increment	xx	xx	xx	data (8)	n	04h
Load Timebase	xx	xx	data (16)		n	06h
Load Velocity	xx	data (24)			n	07h
Load Preset ON Value	data (32)				m	0Bh
Enable/Disable Preset ON Interrupt	xx	xx	xx	data (8)	m	0Fh
Load Preset OFF Value	data (32)				m	15h
Enable/Disable Preset OFF Interrupt	xx	xx	xx	data (8)	m	19h
Load Preload Value	data (32)				n	1Fh
Load Oscillator Divider	xx	xx	data (16)		0	32h

m = Preset Number (1 to 4); n = Counter Number (1 or 2);

xx = Do not care (ignored); data (8, 16, 24, 32) = 8, 16, 24, or 32 bit data

Descriptions of each command are given below. The valid range of values is given in parenthesis.

Null

This is the default %AQ data command. Since the %AQ data is transferred each PLC sweep, it is a good idea to have the Null command present when not executing a specific data command to avoid inadvertent execution. All data is ignored with a Null command.

Load Accumulator Value (Low Limit to High Limit)

This command places a 32-bit value into a counter accumulator. The value must be within the Count Limits, or an error will be returned and the command ignored.

Load High Limit (–2,147,483,648 to 2,147,483,647)

This command sets the highest value to which a counter will count. Counts that would cause the counter to go higher are ignored or cause the accumulator to roll over to the Low Limit depending on whether the counter is configured for Single-shot or Continuous count mode. The High Limit can be any 32-bit value with the following restrictions: it must be greater than the Low Limit, the counter's Preload value must lie between it and the Low Limit, and all preset outputs which are assigned to the counter must have preset ON and OFF values which lie between it and the Low Limit. If a restriction is not met, an error will be generated and the command ignored. If the range between the Low Limit and the new High Limit excludes the Accumulator, the Accumulator will be set to the Low Limit and no error is generated.

Load Low Limit (–2,147,483,648 to 2,147,483,6477)

This command sets the lowest value to which a counter will count. Counts that would cause the counter to go lower are ignored or cause the accumulator to roll over to the High Limit depending on whether the counter is configured for Single-shot or Continuous count mode. The Low Limit can be any 32-bit value with the following restrictions: it must be less than the High Limit, the counter's Preload value must lie between it and the High Limit, and all preset outputs which are assigned to the counter must have preset ON and OFF values which lie between it and the High Limit. If a restriction is not met, an error will be generated and the command ignored. If the range between the new Low Limit and the High Limit excludes the Accumulator, the Accumulator will be set to the Low Limit and no error is generated.

Load Accumulator Increment (–128 to 127)

The Accumulator Increment performs a one-shot adjustment to the accumulator. Only byte 2 is used for data, all other data bytes are ignored. The one-shot increment can be performed at any time, even when counting at maximum rate. If the offset causes the counter to exceed its limits, the excess is treated just like any other overflow, that is., in Continuous mode the Accumulator rolls over to the other limit and in Single-shot mode the Accumulator does not pass the limit.

Load Timebase (1 to 65535 milliseconds)

This command sets the timebase. The timebase is the number of milliseconds for which the counter counts input pulses and then returns in the Counts per Timebase register. If the timebase is 1000, or 1 second, the Counts per Timebase register returns the number of counts detected in each 1 second period. Any non-zero 16-bit value may be used as the timebase.

Load Velocity (–100,000 to 100,000 counts per second)

A velocity increment is an internal count generator, or a continuous accumulator increment. Each millisecond, 0.1% of the increment value is added to the accumulator. A value of 0 will stop the velocity increment. Counts from the velocity increment are cumulative with counts coming in from the Count Pulse input. Note that counts generated by the velocity increment are not reflected in the Counts per Timebase register.

Load ON and OFF Preset Value (Count limits of the assigned counter)

This command sets the preset output turn on and turn off points within a counters range. Preset values can be any value between the high and low limits, inclusive.

Enable/Disable Preset ON and OFF Interrupts (0=Disable, 1=Enable)

This command enables or disables interrupts resulting from Preset output transitions. For example, if Preset ON interrupts are enabled, then a low to high transition of the Preset ON output will generate an interrupt to the CPU. This command allows the interrupts to be enabled or disabled within the ladder program.

Load Preload Value (Low Limit to High Limit)

The Load Preload command sets the value to which the Accumulator will be set when a positive edge occurs on the Preload input. The value must be between the High and Low Limits or an error will be returned and the command ignored.

Load Oscillator Divider (1 to 65535)

This command changes the frequency of the square wave oscillator signal. The frequency generated is 1 megahertz (1 MHz) divided by the oscillator divider. Therefore to get 50 Hz, the oscillator divider is 20000.

Chapter 5 Counter Type C

Counter type C is described in this chapter. The counter description includes counter operation, configuration of the counter, and the interface between the counter and the CPU.

Contents and Operation of a Type C Counter

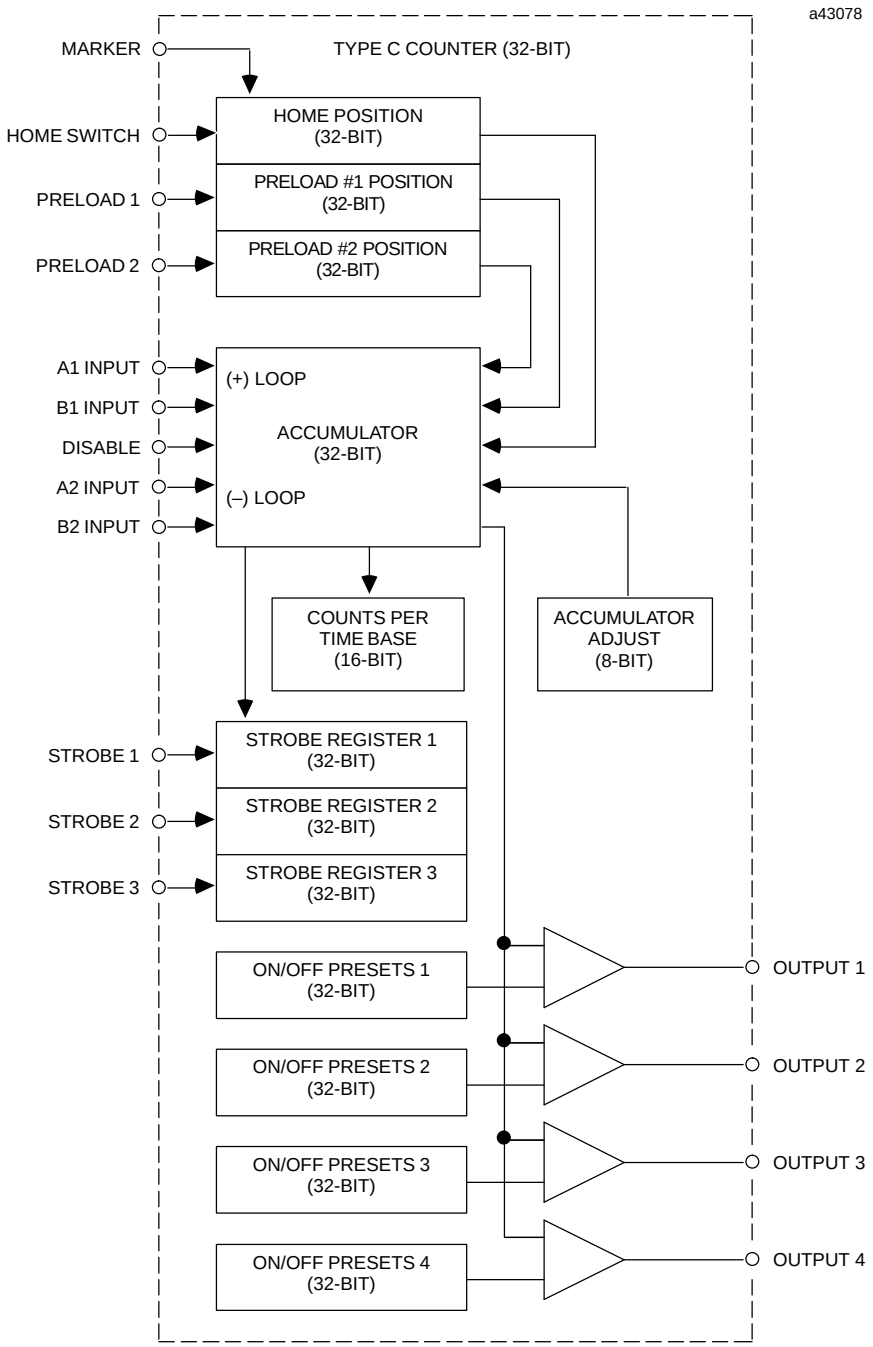
Overview

The Type C counter contains a single, complex 32-bit bidirectional counter. The counter uses 12 single ended or differential voltage inputs: two pairs of count inputs (Count A1, Count B1, Count A2, and Count B2), three independent strobe inputs (Strobe 1, Strobe 2, and Strobe 3), two preload inputs (Preload 1 and Preload 2), Disable, Home Switch, and Marker. The counter may be configured to count in one of three modes: Up and Down, Pulse with Direction, and A Quad B. Counter type C elements are shown in the figure below.

The counter has a 32-bit accumulator register which sums the pulses from a positive input loop and a negative input loop, a Disable input which causes the accumulator to ignore pulses on the input loops, three strobe registers which store the Accumulator value when a corresponding Strobe input transitions, two preload values of which one is inserted into the accumulator the corresponding preload occurs, a Home value which is inserted into the accumulator when a Home Cycle occurs, and a counts per timebase register which indicates the count rate of the input pulses.

The positive input loop is made up of Count A1 and Count B1, and the negative input loop is made up of Count A2 and Count B2.

Each of four Presets is tied to one of the four 5 to 30 V outputs and can be used to generate PLC interrupts.



Count Inputs and Accumulator

The 32-bit Accumulator is incremented or decremented based on a configured interpretation of the two pairs of count inputs that can be connected to operate in a differential fashion. The accumulator sums the inputs from the positive and negative input loops.

Type C Counter Positive and Negative Loops

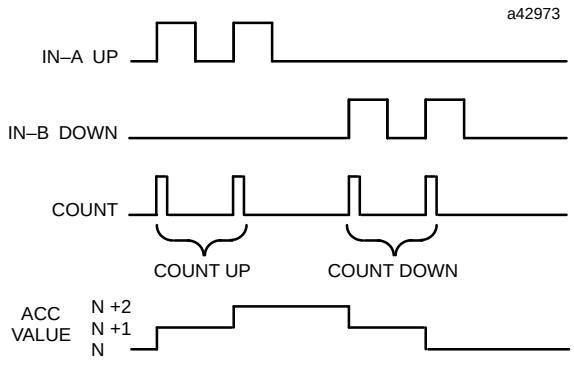
In the Type C counter configuration, pulses on the positive loop are counted normally, while pulses on the negative loop are inverted. The following table describes the accumulator function for the different input loop combinations.

Count Direction		ACCUMULATOR FUNCTION x = counts on (positive) loop y = counts on (negative) loop
(positive) Loop A1, B1	(negative) Loop A2, B2	
Up	Up	Differential (x–y)
Up	Down	Additive (x+y)
Down	Up	Additive –(x+y)
Down	Down	Differential (y–x)
Up	no connection	Counts Up (x)
Down	no connection	Counts Down (–x)
no connection	Up	Counts Down (–y)
no connection	Down	Counts Up (y)

The interpretation for each input loop can be set to Up / Down, Pulse / Direction, or A Quad B. Note that the direction is reversed for the negative loop. Each is described below.

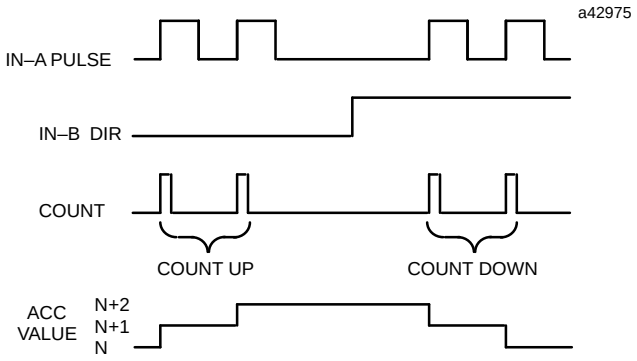
Operating in UP/DOWN Mode

Up-counting occurs on the low-to-high transition of the Up input. Down counting occurs on the low-to-high transition of the Down input.



Operating in Pulse/Direction Mode

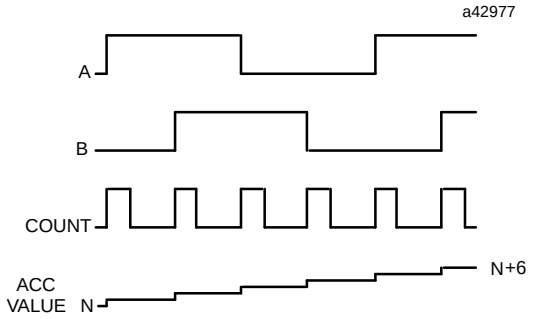
Counting always occurs on the low-to-high transition of the Pulse input. Count direction is up for a low level on the Direction input and down for a high level on the Direction input. Avoid changing the DIR signal coincidentally with the rising edge of the Pulse input.



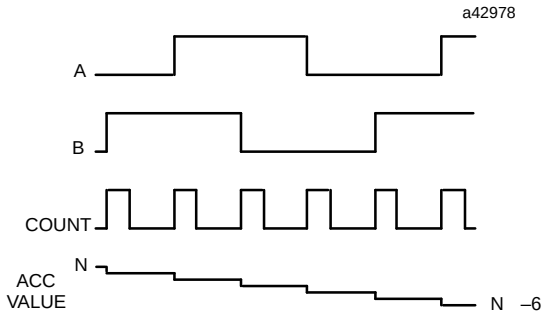
Operating in A Quad B Mode

In A Quad B mode, there are four counts for each A Quad B cycle. A count occurs for each transition of either A or B. The counts will be evenly spaced with respect to the input waveforms when the phase relationship between A and B is shifted by 1/4 cycle. The phase relationship between A and B determines count direction, as shown in the following timing diagrams.

The count direction is up if A leads B.

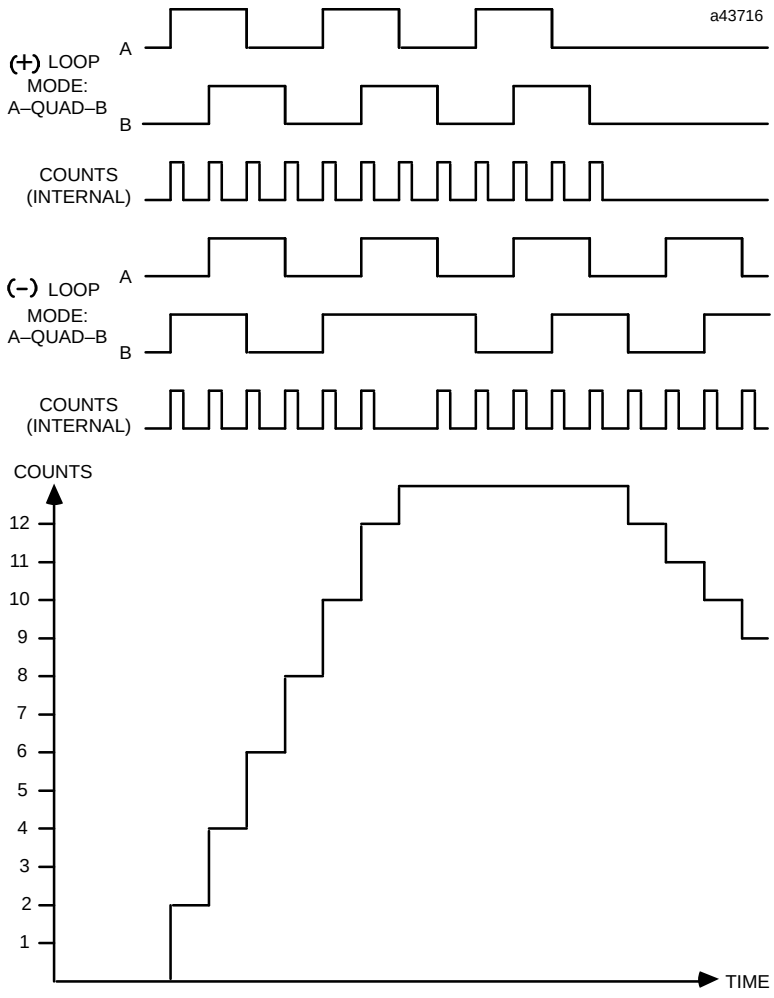


The count direction is down if A lags B.



Differential Counting

Operation of the Accumulator in a typical differential application is illustrated below.



The Accumulator is bounded by configurable High and Low Limits. The interaction between the Accumulator and the limits depends on the configured count mode. In Continuous mode, the Accumulator will increment or decrement to the current High or Low Limit, roll over to the other limit, and continue counting. In Single Shot mode, the Accumulator will count to the current High or Low Limit and stop. If the counter direction is changed, the Accumulator will count away from the limit until it reaches the other limit.

The High and Low Limits can be changed to any valid 32-bit value at any time using a data command from the PLC. To be a valid 32-bit value, the following conditions must be met:

- the High Limit must be greater than the Low Limit
- both Preload values must be within the High and Low Limit bounds
- the Home value must be within the High and Low Limit bounds
- all presets must be within the High and Low Limit bounds

If the limits are changed so the Accumulator is outside the limit boundaries, the Accumulator is set to the Low Limit.

The Accumulator may be set to any 32-bit value within the bounds of the High and Low limits at any time using a data command. Another data command allows the Accumulator to be adjusted by a byte value, from –128 to +127. Finally, a velocity increment can be commanded which causes the Accumulator to increment or decrement at a fixed rate.

Strobe Inputs and Register

Each Strobe input is an edge sensitive input which can be configured to respond to either a positive edge or a negative edge. When the configured Strobe input transition occurs, (referred to as a Strobe Pulse) the value in the Accumulator is stored in the corresponding Strobe register and a strobe flag is set and returned in %I data to indicate the event to the CPU. The application program in the CPU acknowledges receipt of the strobe by toggling the corresponding Reset Strobe %Q bit.

Two strobe modes are available to select which Strobe value is most important. **In Last Strobe mode, the default, a Strobe Pulse will always update the Strobe register with the latest Accumulator value regardless of the strobe flag state.** In First Strobe mode, the first strobe value is captured and all subsequent Strobe Pulses are ignored until the strobe flag is cleared by toggling the corresponding %Q bit.

Preload Input and Value

The Preload input is normally used to perform a reset function for the counter. The value to which the Accumulator is set when a preload occurs can be configured to any 32-bit value within the range of the high and low limits and has a default value of zero. The Preload value can also be changed using a data command from the PLC. There are two types of preloads, hardware and software.

The Preload input is positive edge sensitive only. On the positive transition, the configured preload value is inserted into the accumulator and a preload flag is set and returned in %I data to indicate the event to the CPU. If an application program uses this flag indication, it may use the corresponding %Q bit to clear the preload flag before the next preload occurs. **A rising edge on the Preload input always preloads the Accumulator regardless of the state of the Preload flag.** Preload 1 has precedence over Preload 2 when both occur simultaneously.

Note that when a Preload pulse occurs on the inputs at the same time as a Strobe pulse, or if the inputs are tied together, the Preload has precedence. The Accumulator will be set to the Preload value and then the Strobe register will be set to the Accumulator. Thus the Strobe register will obtain a copy of the Preload value.

A software preload can be performed by setting a Preload Accumulator %Q bit. On the positive transition of this %Q bit, the preload value is placed into the Accumulator. A software preload does NOT set the Preload Status flag. Note that there are two Preload Accumulator %Q bits in a Type C counter, each with its own Preload value.

Home Switch, Marker Input, and Home Value

The Marker input is used in conjunction with the Home Switch to perform a homing function for the counter. The value to which the Accumulator is set when a Home Cycle completes can be configured to any 32-bit value within the range of the high and low limits and has a default value of zero. The Home value can also be changed using a data command from the PLC.

A Home Cycle is started by setting the Home Command %Q bit. Once the Home Cycle starts, a rising edge on the Marker input while the Home Switch is level high will complete the Home Cycle and place the Home value into the Accumulator. A Home Found flag is set and returned in %I data to indicate the event to the CPU. The Home Found flag will remain set until the next rising edge of the Home Command %Q bit.

The Home Cycle has precedence over the two preloads and the Accumulator value will contain the Home value if a Home Cycle completes simultaneously with any Preload input rising edge.

Counts per Timebase Register

The Counts per Timebase register is a 16-bit register which contains the number of counts received in the last completed timebase interval. It is used to measure the rate of counting. If more counts are received than can be stored in a 16-bit register, the register will overflow. The timebase interval is a configurable value from 1 to 65535 milliseconds.

Changes to the timebase will not take effect until after the previous timebase and one new timebase have elapsed. A Preload will interrupt counting and will cause the Counts per Timebase register to be inaccurate for up to two timebase intervals. The timebase is initially configured as 1 second, but may be changed using the Logicmaster 90-70 Configurator function or a data command.

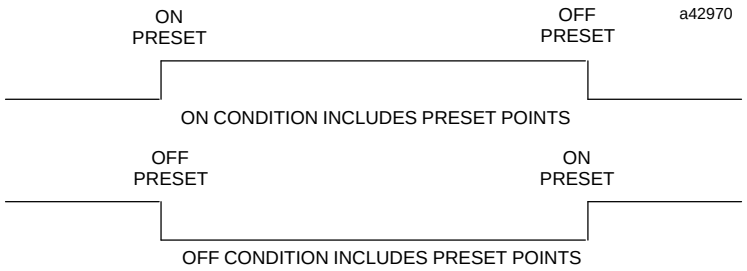
As an unsigned number, the Counts per Timebase register will correctly indicate from 0 to 65536 positive counts received per timebase. As a signed number, it will properly indicate from –32768 to 32767 counts per timebase. The timebase should be selected to not allow more counts in a timebase than the 16-bit register can hold or it will overflow.

Preset Outputs

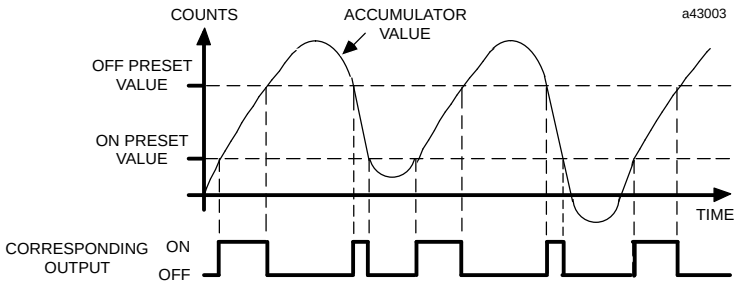
The module has four preset outputs. Each preset output has a preset ON and preset OFF value, or position, which must be within the count limits. The preset ON and OFF positions determine when the output will be ON or OFF.

Preset closest to low limit	Output ON	Output OFF
ON	> = ON Preset < = OFF Preset	> OFF Preset < ON Preset
OFF	< OFF Preset > ON Preset	< = ON Preset > = OFF Preset

The output may be either on or off when the accumulator value lies between the Preset points.



For example:



Separation of Preset Points

The count accumulators are compared to the Presets at 0.5 msec intervals. Therefore, to guarantee that the outputs will always switch, the Preset points must be separated by at least the number of counts received in a 0.5 msec time period. For example:

If maximum count rate = 10kHz;
then minimum count separation = (10,000 Hz x .0005 sec) = 5 counts.

Preset Interrupts

Interrupts can be enabled or disabled for each preset output's ON and OFF transition. At the same time a preset output changes state, the CPU is interrupted. %I and %AI input data are updated so that an interrupt routine will see the most current data from the High Speed Counter. From the %I data, an interrupt routine can determine which presets changed state and which edge(s) generated the interrupt. Simultaneous preset changes generate only 1 interrupt to the CPU. Once configured, interrupts can be independently enabled or disabled using data commands. See Appendix B for information on using the interrupt capability.

Output Failure Mode

When the CPU is stopped or lost, counter operation continues normally without interfacing to the CPU. Until the CPU returns or power is cycled, the operation of the Preset outputs can be configured. In Normal mode, the outputs continue to operate as if the CPU were present. Outputs will change state to reflect the counter Accumulator. In Force Off mode, all preset outputs are turned off and remain off until the CPU returns.

In Holdlast mode, the preset outputs retain current levels and do not reflect the counter Accumulator. If the CPU returns to operation, the outputs will immediately begin reflecting the counter Accumulator.

Oscillator Output

The High Speed Counter module generates a 5V square wave oscillator signal. The oscillator output frequency is determined by the current oscillator divider (set in configuration or by data command) as indicated below:

Oscillator Frequency (Hz) = 1,000,000 Ï oscillator divider

The output frequency ranges from approximately 15 Hz (oscillator divider of 65535) to 1 MHz (oscillator divider of 1).

Table 5-1. Type C Specific Terminal Strip Assignments

Pin	Signal Name	Type C Pin Name	Type C Pin Description
1,3	IN1	COUNT INPUT A+	Count positive loop A input
2,4	IN2	COUNT INPUT B+	Count positive loop B input
5,7	IN3	COUNT INPUT A–	Count negative loop A input
6,8	IN4	COUNT INPUT B–	Count negative loop B input
11,13	IN5	PRELOAD1	Counter preload 1 input
12,14	IN6	DISABLE1	Counter disable input
15,17	IN7	PRELOAD2	Counter preload 2 input
16,18	IN8	HOME	Home switch input
21,23	IN9	STROBE 1	Counter strobe 1 input
22,24	IN10	STROBE 2	Counter strobe 2 input
25,27	IN11	STROBE 3	Counter strobe 3 input
26,28	IN12	MARKER	Encoder marker input

Configuring the Type C High Speed Counter

The following table summarizes all configuration features and default configuration values for the Type C counter.

Configuration Parameter	Description	Values	Default
Failure Mde	Output Failure Mode	NORMAL, OFF, HOLD	NORMAL
Osc Divider	Oscillator Divider	1 ... 65535	1000
Count Thrshlds	Count Input Thresholds	NON-TTL, TTL, MAG-PKUP	NON-TTL
Control Thrshlds	Control Input Thresholds	NON-TTL, TTL	NON-TTL
Count Filtr	Count Input Filter	HIFREQ, LOWFREQ	HIFREQ
Preld Filtr	Preload Input Filter	HIFREQ, LOWFREQ	HIFREQ
Disbl Filtr	Disable Input Filter	HIFREQ, LOWFREQ	HIFREQ
ON	Preset ON Setpoint	Low Limit ... High Limit	8,388,607
OFF	Preset OFF Setpoint	Low Limit ... High Limit	0
ON Interrupt	Preset on transition interrupt	DISABLED, ENABLED	DISABLED
OFF Interrupt	Preset off transition interrupt	DISABLED, ENABLED	DISABLED
Hi Limit	High Count Limit	–2,147,483,648 ... 2,147,483,647	8,388,607
Lo Limit	Low Count Limit	–2,147,483,648 ... 2,147,483,647	0
Count Mode	Count Mode	CONTINU, SINGSHOT	CONTINU
Count Sig	Count Signals	PULSE / DIR, UP / DOWN, A QUAD B	PULSE / DIR
Timebase(ms)	Timebase	1 ... 65535 ms	1000 ms
Preld 1 Value	Preload 1 Value	Low Limit ... High Limit	0
Preld 2 Value	Preload 2 Value	Low Limit ... High Limit	0
Home Value	Home Value	Low Limit ... High Limit	0
Strobe Mode	Strobe Mode	LAST, FIRST	LAST
Strobe 1 Edge	Strobe 1 Edge	POS, NEG	POS
Strobe 2 Edge	Strobe 2 Edge	POS, NEG	POS
Strobe 3 Edge	Strobe 3 Edge	POS, NEG	POS

Output Failure Mode

When the CPU is stopped or lost, counter operation continues normally, however, the operation of the Preset outputs until the CPU returns or power is cycled can be configured. In all modes, the Accumulator is updated and the Strobes, Preloads, and Home Cycle are processed normally.

In Normal mode (NORMAL), the outputs continue to operate as if the CPU were present. Outputs will change state to reflect the counter Accumulator.

- In Force Off mode (OFF), all preset outputs are turned off and remain off until the CPU returns.
- In Holdlast mode (HOLD), the preset outputs retain current levels and do not reflect the counter Accumulator.
- If the CPU returns to operation or the module is power-cycled, the outputs will immediately begin reflecting the counter Accumulator again.

Oscillator Divider

The oscillator divider is used to generate a 5V oscillator output. The output frequency is 1 million divided by the oscillator divider; the formula is shown below.

Oscillator Frequency (Hz) = 1,000,000 / oscillator divider

The output frequency ranges from approximately 15 Hz (oscillator divider of 65535) to 1 MHz (oscillator divider of 1).

Input Thresholds

All inputs can be used as differential or single-ended inputs. The following table specifies the input thresholds for single-ended and differential use based on threshold selection and input type. The configuration parameters will set input thresholds according to the following table:

Configuration Parameter	Inputs Controlled	Input Definitions
CounterThreshold	IN1, IN2, IN3, IN4	Count Pulse 1A, 1B, 2A, 2B
ControlThreshold	IN5, IN6, 1N7, 1N8, IN9, IN10, 1N11, 1N12	Preload 1, Preload 2, Disable, Strobe 1, Strobe 2, Strobe 3, Marker, Home Switch

Note that all the inputs controlled will have the same voltage threshold.

The voltage thresholds which can be selected for each input are described in the following table.

Input Type	Single-Ended			Differential		
	Non-TTL	TTL	Mag-Pickup	Non-TTL	TTL	Mag-Pickup
CounterThreshold	8 V	1.4 V	0.1 V	4.8 V	0.8 V	0.1 V
ControlThreshold	8 V	1.4 V	X	4.8 V	0.8 V	X

Input Filters

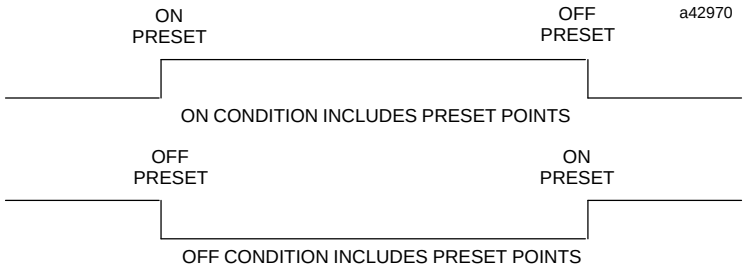
All inputs default to using a 2.5 microsecond high-frequency filter. Each Preload, Disable, and pair of Count inputs can be configured to use a 12.5 millisecond low-frequency filter instead. The low-frequency filter reduces the effects of signal noise. The Strobe, Marker, and Home Switch inputs always use the high-frequency filter.

Output Preset ON and OFF Positions

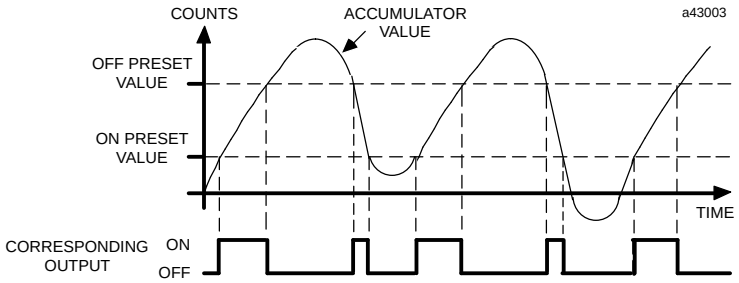
Each counter output has a preset ON and OFF position. The output state indicates when the counter accumulator value is between the ON and OFF points.

Preset closest to low limit	Output ON	Output OFF
ON	> = ON Preset < = OFF Preset	> OFF Preset < ON Preset
OFF	< OFF Preset > ON Preset	< = ON Preset > = OFF Preset

The output may be either on or off when the accumulator value lies between the Preset points.



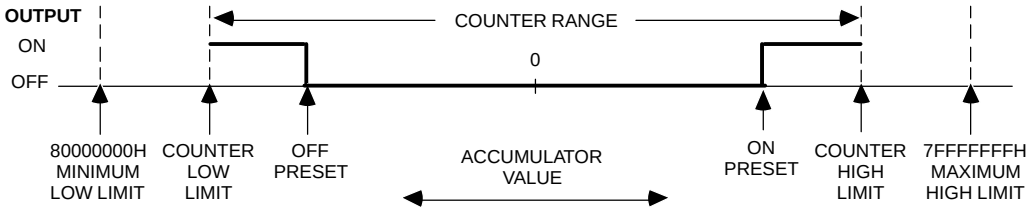
For example:



Location of Preset Points

The Preset points may be located anywhere within the counter range. When the accumulator value is between the Preset points, the output ON / OFF state will always be that of the lowest (most negative) Preset point. When the accumulator value is *not* between the Preset points, the output ON / OFF state will be that of the most positive preset. This is true regardless of the counter direction.

The following example compares the output state and accumulator value of a 32-bit counter.



If both preset points are within the counter range, the output always switches at the Preset points. If only one of the Preset points is programmed within the counter range, then the counter limits will function as the other Preset point. In the continuous mode, the output will switch when wraparound occurs.

If neither of the Preset points is in the counter range then the output state will not change; it will always be the state of the most positive Preset. If both Preset points are equal and out of range, the output will always be OFF. If both Preset points are equal

and within the counter range, then the output will only be on for one count value - as defined by the Preset points.

Preset Interrupt Enables

Each preset can generate an interrupt to the CPU. If the Interrupt ON selection is enabled, then an ON transition of the preset output will generate an interrupt to the CPU. Similarly, if the Interrupt OFF selection is enabled, an OFF transition of the preset output will generate an interrupt to the CPU. Thus no edge, either edge, or both edges of a preset output transition can generate an interrupt. The default is for all interrupts to be disabled.

Count Limits

Each counter is assigned upper and lower count limits. The upper (high) limit must the most positive, and the lower limit must be the most negative. Both limits can be positive or negative, but the high limit must always be greater than the low limit. The Accumulator, Preload values, Home Value, and all Preset outputs must lie within the high and low limits.

If the Accumulator value is outside the new limits when the limits are changed it is automatically adjusted to the low limit value. If the new limits are incompatible, that is, (high < low or Low > high), then they will be rejected and the old limits retained. In this case a counter limit error code will be returned. To avoid this situation when the limits are changed one at a time, a good rule to follow is: always move the high limit first when shifting the limits up and always move the low limit first when shifting them down.

As a 32-bit counter, the limit range is –2,147,483,648 to 2,147,483,647.

Count Mode

A counter can be configured to count continuously within the count limits, or to count to a limit and stop.

Continuous Counting

In the continuous counting mode, if either the upper or lower limit is exceeded, the counter wraps around to the other limit and continues counting. Continuous counting is the default mode.

Single-Shot Counting

If single-shot is selected, the counter will count to its upper or lower limit, then stop. When the counter is at the limit, counts in the opposite direction will count it back off the limit. The Accumulator can also be changed by loading a new value from the CPU or by applying a Preset Input.

Count Signal Mode

Each pair of count inputs can be configured to interpret signals in one of three ways:

- Up / Down mode mode - rising edges on the A, or up, input increment the Accumulator while positive transitions on the B, or down, input decrement the Accumulator.
- Pulse / Direction mode - rising edges on the A, or pulse, input are counted. If the B, or direction, input is low then the Accumulator is incremented but if the Second input is high then the Accumulator is decremented.
- A Quad B mode - if the A input leads the B input, the Accumulator is incremented and if the B input leads the A input the Accumulator is decremented.

Counter Timebase

For each counter, the timebase represents a span of time which can be used to measure the rate of counting. For example, a program required to monitor the number of count pulses which occur every 30 seconds could use a timebase of 30,000.

A timebase from 1 millisecond to 65535 milliseconds can be selected for each counter. The counter timebase is set to 1 second (1000 milliseconds) by default. The module stores the number of counts that occurred during the last-completed timebase interval in theCounts / Timebase register.

The timebase counter updates once each timebase period. After power-up, or any disruption in counting, allow at least one timebase period for the counter to stabilize.

Preload Value

For each counter, a starting, or Preload, value can be specified which will be used when the Preload input is activated. This Preload value is used for both hardware and software preloads. If the counter should be reset to zero, enter 0 as the Preload value; this is the default value. The Preload value range is –2,147,483,648 to +2,147,483,647, but it must be within the counter limits.

Home Value

If the module has been set up to operate as a Type C counter, a Home Value can be selected. The default for the Home Value is 0. The counter will be set to this value when all three of the following events occur:

1. Find Home command is given by the CPU;
2. Home Switch input is present;
3. next Marker input pulse occurs.

Additional markers will be ineffective until the Home Command is removed and the Home Command sequence is repeated. If the Home Command is removed before the Home marker is found, a ***Home Error*** will be returned.

Strobe Mode

The Strobe Mode determines which Strobe input pulse the Strobe register will report. In Last mode, the Strobe register is always updated with the Accumulator value when the configured Strobe input transition occurs. Thus two rapid Strobe pulses could result in the first Strobe register value being missed. In First mode, the Strobe register is updated only if the Strobe flag set by a previous Strobe pulse has been acknowledged by setting the corresponding Reset Strobe %Q bit. In this mode, any subsequent Strobe pulses will be ignored and lost, but the first will always be retained. The default mode is Last.

Strobe Edge

Strobe inputs are edge sensitive. Each Strobe input on the module can be individually configured to have either the positive or the negative edge active. By default, they are positive-edge sensitive.

Data Transfer Between High Speed Counter and CPU

The Series 90-70 High Speed Counter updates the %I and %AI data every 0.5 milliseconds. The Series 90-70 CPU reads this data immediately preceding every pass through the ladder logic, before triggering a ladder interrupt, and when a DOIO specifically requesting this data is performed in the ladder logic. To support the unique data coherency requirements of the High Speed Counter, the CPU reads both the %I and %AI data when performing DOIOs requesting only %I data.

The format of this input data depends on the counter configuration type. In return, during each I/O scan, the CPU sends 32 bits (%Q) of control data and 6 words (%AQ) of output data commands to the module. COMMREQ function blocks in the user program can be used to send additional data commands to the module.

See Appendix A for more information about the COMMREQ and DOIO functions.

%I and %AI Data Sent by a Module Configured as Type C

The 32 status bits (%I) represent:

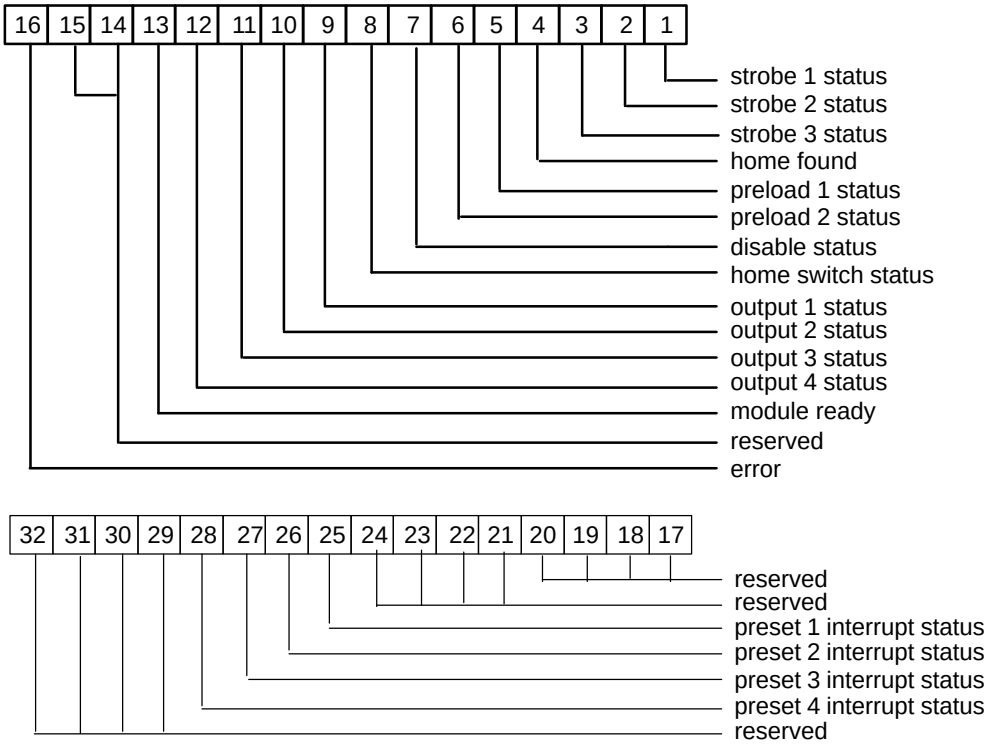
- Strobe status flag
- Preload status flag
- Disable status
- Preset Output status
- Module ready status
- Home Switch status
- Error status

These status bits are sent to the CPU as inputs, and can influence outputs sent from the CPU to the module.

The 16 register data words (%AI) represent:

- Counts per Timebase value
- Accumulators
- Strobe Registers
- Module Status Code

Status Bits (%I) - Type C Counter



Strobe Status

Each bit indicates when a Strobe Pulse occurs on the counter. If an application program uses this bit, it should be cleared by setting the corresponding Reset Strobe %Q bit. In First Strobe mode, additional strobes will be ignored until the Reset Strobe %Q bit is set.

Home Found

This bit indicates the completion of the Home Cycle. It is set on the rising edge of the Marker input when the Home Switch is ON and the Find Home %Q bit is set. When the Find Home %Q bit is cleared and then set again, the Home Found bit is cleared.

Preload Status

Each bit indicates a rising edge of the corresponding Preload input on the counter. If an application program uses these bits, it should clear them by setting the corresponding Reset Preload %Q bit.

Disable Status

This bit indicates the level of the Disable input and whether counting is disabled. When set, the Disable input is ON and count inputs are ignored.

Home Switch Status

This bit indicates the level of the Home Switch input. When set, the Home Switch input is ON. The Home Switch is often used in positioning applications to indicate which side, in reference to a Home Position, or a range close to a Home Position.

Output Status

These bits indicate the ON or OFF state of the four preset outputs.

Module Ready

This bit is set after the module completes its power-up tests.

Error Status

This bit is set when an error occurs. If it is set, a module status code has been returned in the first %AI location and the board OK light is flashing. The Error Status bit is cleared by setting the Clear Error %Q bit.

Preset Interrupt Status

These bits are set by the HSC when the corresponding preset output has changed state, generating an interrupt. These flags may be used by an interrupt routine to indicate which counters have generated interrupts. The Output Status bits can be used in conjunction to determine which transition caused the interrupt. The Preset Interrupt Status bits should only be tested in a ladder interrupt handler.

%AI Data - Type C Counter

Word	Description
01	Module Status code
02	Counts per timebase for counter 1
03	Not used (set to 0)
04-05	Accumulator for counter 1
06-07	Strobe register 1
08-09	Strobe register 2
10-11	Strobe register 3
12-16	Not used (set to 0)

Module Status Codes

The Module Status Code in the %AI Input Data contains the error code returned to the PLC. The HSC sets this code to indicate a data command or configuration error. Once an error code has been returned, no more errors will be generated until the error is cleared. To clear a module status code, eliminate the condition that caused the error (for example, clear the %AQ command data, or clear the Home Command %Q bit), and toggle the Clear Error %Q bit.

Note that fatal errors (RAM, EPROM) have no codes associated with them because these errors cause the watchdog timer to time out and the board to go into constant reset.

The error code format and a list of error codes are given below.

High Byte		Low Byte
Error Source	Counter or Preset #	Error Code

Error Codes for Type C

Error Code	Error Type	Definition
00	No Error	No Error Present
04	Command Errors	Home Error
11		Unknown Command
21		Invalid Counter or Preset
31		Invalid COMMREQ Task ID
41		Velocity Increment Out of Range
81		Accumulator Out of Range
91		Preload 1 Value Out of Range
A1		Preload 2 Value Out of Range
A1		Preload 2 Value Out of Range
B1		Home Value Out of Range
C1		Preset On Out of Range
D1		Preset Off Out of Range
12	Limit Errors	High Limit < Low Limit
22		Range Excludes Preload 1 Value
32		Range Excludes Preload 2 Value
42		Range Excludes Home Value
52		Range Excludes Preset ON
62		Range Excludes Preset OFF
18	Configuration Errors	High Limit < Low Limit
28		Range Excludes Preload 1 Value
38		Range Excludes Preload 2 Value
48		Range Excludes Home Value
58		Range Excludes Preset ON
68		Range Excludes Preset OFF
A8		Unsupported Feature Error
B8		Unknown Counter Type
C8		PLC Version Error
D8		Logicmaster 90 Version Error

Configuration Errors are not returned in %AI data since the module does not configure, but the error code is returned in the IO Fault data.

Counter or Preset Number

For a valid command (recognized value in byte 0), the counter or preset number which generated the error will be reported in this nibble. In counter Type C, the counter number is always 1. A preset number only appears in error codes C1 and D1.

Error Source

Command and Limit errors return the source of the error.

Value	Error Source
1	%AQ Command 1 (%AQ Offset 0-2)
2	%AQ Command 2 (%AQ Offset 3-5)
4	COMMREQ Function

Example:

If the hexadecimal data 0002 0000 0107 was placed into the %AQ offsets 3 through 5, the error 2141h would be reported. The Module Status Code represents:

Value	Representation
2	Error in %AQ Command 2
1	Error generated by counter 1
41	Velocity Increment Out of Range

%Q and %AQ Data Sent from CPU to HSC Configured as Type C

Once each I/O scan, the CPU sends eight words of data (32 bits of %Q and six words of %AQ) to the High Speed Counter Module. The application program can use these outputs to send commands to the module.

The 32 output bits (%Q) represent:

- Reset Strobe flag
- Reset Preload flag
- Clear error flag
- Output enable
- Home command
- Preload Accumulator

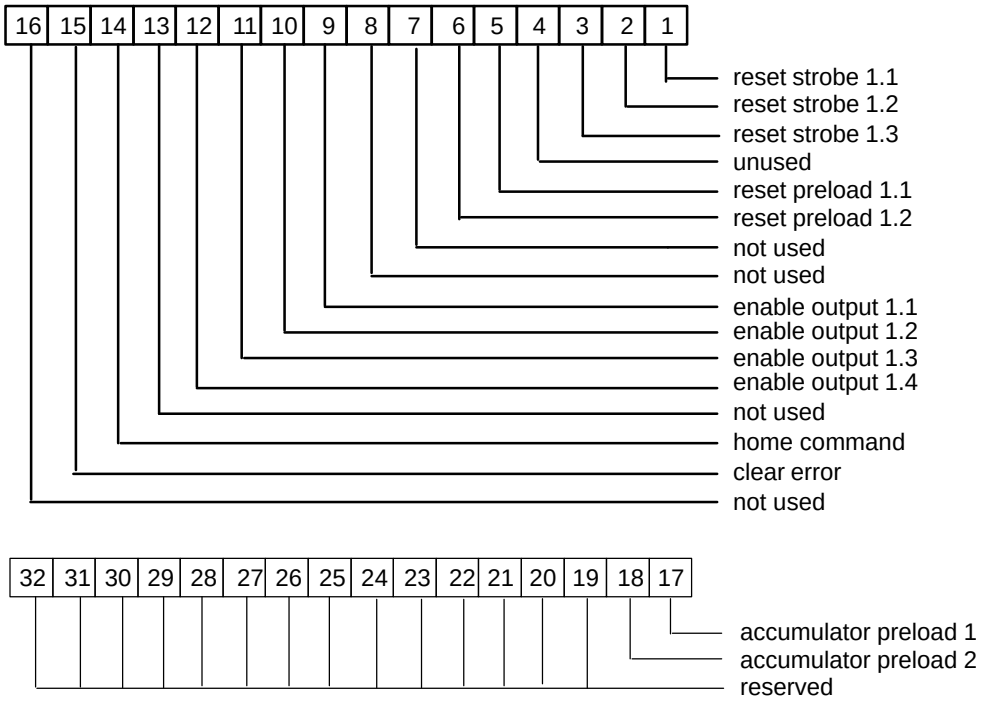
All of this data is transferred from the High Speed Counter to the CPU once per I/O scan. The I/O scan is active while the CPU is in the RUN mode or STOP ENABLED mode.

Six Words (%AQ) of Command Data

The 6 words of command data, which can also be sent using a COMMREQ Function Block, can perform the following operations:

- Load Accumulator
- Load count limits
- Load Accumulator increment
- Load output preset ON and OFF values
- Load Preload
- Load time base
- Load Oscillator divider
- Count Direction
- Enable/Disableinterrupts

%Q Data - Type C Counter



Reset Strobe

Setting this bit clears the corresponding Strobe Status %I bit. In First Strobe mode, subsequent strobe pulses are ignored until this bit is used to clear the Strobe Status bit.

Reset Preload

This bit is used to clear the corresponding Preload Status %I bit. For example, if a Preload 2 occurred, the Preload 2 Status %I bit would be set. To clear this bit so future Preloads can be detected, the Reset Preload 2 %Q bit must transition ON.

Enable Output

These bits enable the corresponding preset output. If cleared, the output will always be OFF and not reflect the accumulator's value in relation to the Preset ON and OFF values.

Home Command

This bit is used to start a Home Cycle. When this bit transitions ON, the Home Switch and Marker inputs are monitored. When the Home Switch is set and a rising edge occurs on the Marker input, the Accumulator is set to the Home value and the Home Found %I bit is set. If the Home Command bit is cleared before the Home Found bit is set, a Home Error occurs.

Clear Error

This bit should be set by the CPU to clear the Error Status %I bit after the error has been acknowledged. This bit is rising edge active, so new errors may appear while set.

Preload Accumulator

These bits cause the counter to perform a software preload and set the corresponding Accumulator to the Preload value. The Preload Status bit is not set when a software preload is performed.

Data Commands for Counter Type C

The High Speed Counter provides six %AQ words to send data commands from the PLC to the HSC. The first three words, offsets 0 through 2, make up %AQ command 1, and the second three words, offsets 3 through 5, make up a completely separate %AQ command 2. Thus two commands can be sent to the HSC at the end of each sweep. Note that %AQ command 1 is executed first, so that if identical commands with different values are sent to the HSC simultaneously, %AQ command 2 data will overwrite %AQ command 1 data.

Even though the %AQ data is sent each sweep, commands are acted on ONLY if the command has changed since the last sweep. When any of the 6 bytes in a command changes, the HSC will accept the data as a new command and respond accordingly.

The DOIO function is supported, so that data can be transferred between the CPU and HSC mid-sweep. Note that to ensure that the High Speed Counter has time to process DOIO data sent to it, the application should not change the data more frequently than every 0.5 millisecond. Because data sent to the HSC is updated at the end of the CPU sweep, half a millisecond should elapse between the beginning of the sweep and a DOIO function block, between two DOIO function blocks, and between a DOIO function block and the end of the sweep.

The COMMREQ function block can also be used to send data commands to the HSC mid-sweep. COMMREQs must be separated only from each other, and by at least 0.5 milliseconds. A description and example of the use of COMMREQs is given in Appendix A.

%Q data is processed by the HSC before the %AQ data. Therefore commands that can be affected by %Q bit operations should be sent at least one sweep before the %Q bit operation. For example, the Load Preload Value command should be sent one sweep before setting the Preload Accumulator %Q bit to preload that value.

The High Speed Counter will check each command that is sent for validity. If the command syntax is incorrect, the counter will ignore the command and respond by flashing the Board Okay LED at 4 Hz, setting the Error Status %I bit, and returning a status code describing the error in the Module Status %AI word. The Error can be cleared by toggling the Clear Error %Q bit.

In describing data commands, word offsets are shown in reverse order and in hexadecimal to simplify data entry. The following example sends a Load Accumulator Counts command with value 0001 to counter 2 using offsets 0 through 2.

The first word, or command word, which goes into word offset 0 would be 0201h. The value 01 in byte 0 represents the command Load Accumulator Value. The value 02 in byte 1 is the counter number, in this case counter 2. For the Load Accumulator Value command, word 1 is the sixteen bit value to be loaded into the accumulator and word 2 is ignored. In this example, word 1 would have the value 0001h because that is the value to be placed in the accumulator. Word 2 will be ignored and can be anything, but it is usually best to use the value 0. If word offset 0 corresponded to %AQ1, the complete command to load the counter 2 accumulator with value 0001 would be:

%AQ3 (word 2)	%AQ2 (word 1)	%AQ1 (word 0)
0000	0001	0201

The following table is a list of data commands for counter Type C. Byte 0 data is in hexadecimal. Note that since there is only one counter, byte 1 always contains value 1 for the counter number.

Command Definition	Data				Command Word	
	Word 2		Word 1		Word 0	
	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
Null	xx	xx	xx	xx	xx	00h
Load Accumulator Value	data (32)				1	01h
Load High Limit	data (32)				1	02h
Load Low Limit	data (32)				1	03h
Load Accumulator Increment	xx	xx	xx	data (8)	1	04h
Load Timebase	xx	xx	data (16)		1	06h
Load Velocity	xx	data (24)			1	07h
Load Home Value	data (32)				1	08h
Load Preset ON Value	data (32)				m	0Bh
Enable / Disable Preset ON Interrupt	xx	xx	xx	data (8)	m	0Fh
Load Preset OFF Value	data (32)				m	15h
Enable / Disable Preset OFF Interrupt	xx	xx	xx	data (8)	m	19h
Load Preload 1 Value	data (32)				1	1Fh
Load Preload 2 Value	data (32)				1	20h
Load Oscillator Divider	xx	xx	data (16)		0	32h

m = Preset Number (1 to 4);

xx = Do not care (ignored); data (8, 16, 24, 32) = 8, 16, 24, or 32 bit data

Descriptions of each command are given below. The valid range of values is given in parenthesis.

Null

This is the default %AQ data command. Since the %AQ data is transferred each PLC sweep, it is a good idea to have the Null command present when not executing a specific data command to avoid inadvertent execution. All data is ignored with a Null command.

Load Accumulator Value. (Low Limit to High Limit)

This command places a 32-bit value into a counter accumulator. The value must be within the Count Limits, or an error will be returned and the command ignored.

Load High Limit. (–2,147,483,648 to 2,147,483,647)

This command sets the highest value to which a counter will count. Counts that would cause the counter to go higher are ignored or cause the accumulator to roll over to the Low Limit depending on whether the counter is configured for Single-shot or Continuous count mode. The High Limit can be any 32-bit value with the following restrictions: it must be greater than the Low Limit, the counter's Preload value must lie between it and the Low Limit, and all preset outputs which are assigned to the counter must have preset ON and OFF values which lie between it and the Low Limit. If a restriction is not met, an error will be generated and the command ignored. If the range

between the Low Limit and the new High Limit excludes the Accumulator, the Accumulator will be set to the Low Limit and no error is generated.

Load Low Limit. (–2,147,483,648 to 2,147,483,6477)

This command sets the lowest value to which a counter will count. Counts that would cause the counter to go lower are ignored or cause the accumulator to roll over to the High Limit depending on whether the counter is configured for Single-shot or Continuous count mode. The Low Limit can be any 32-bit value with the following restrictions: it must be less than the High Limit, the counter's Preload value must lie between it and the High Limit, and all preset outputs which are assigned to the counter must have preset ON and OFF values which lie between it and the High Limit. If a restriction is not met, an error will be generated and the command ignored. If the range between the new Low Limit and the High Limit excludes the Accumulator, the Accumulator will be set to the Low Limit and no error is generated.

Load Accumulator Increment. (–128 to 127)

The Accumulator Increment performs a one-shot adjustment to the accumulator. Only byte 2 is used for data, all other data bytes are ignored. The one-shot increment can be performed at any time, even when counting at maximum rate. If the offset cause the counter to exceed its limits, the excess is treated just like any other overflow, that is, in Continuous mode the Accumulator rolls over to the other limit and in Single-shot mode the Accumulator does not pass the limit.

Load Timebase. (1 to 65535)

This command sets the timebase. The timebase is the number of milliseconds for which the counter counts input pulses and then returns in the Counts per Timebase register. If the timebase is 1000, or 1 second, the Counts per Timebase register returns the number of counts detected in each 1 second period. Any non-zero 16-bit value can be used as the timebase.

Load Velocity. (–100,000 to 100,000)

A velocity increment is an internal count generator, or a continuous accumulator increment. Each millisecond, 0.1% of the increment value is added to the accumulator. A value of 0 will stop the velocity increment. Counts from the velocity increment are cumulative with counts coming in from the Count Pulse input. Note that counts generated by the velocity increment are not reflected in the Counts per Timebase register.

Load Home Value. (Low Limit to High Limit)

The Load Home command sets the value to which the Accumulator will be set when a Home Cycle occurs. The value must be between the High and Low Limits or an error will be returned and the command ignored.

Load ON and OFF Preset Value. (Low Limit to High Limit)

This command sets the preset output turn on and turn off points within a counters range. Preset values can be any value between the high and low limits.

Enable/Disable Preset ON and OFF Interrupts. (0=Disable, 1=Enable)

This command enables or disables interrupts resulting from Preset output transitions. For example, if Preset ON interrupts are enabled, then a low to high transition of the

Preset ON output will generate an interrupt to the CPU. This command allows the interrupts to be enabled or disabled within a ladder.

Load Preload 1 and 2 Value. (Low Limit to High Limit)

The Load Preload command sets the value to which the Accumulator will be set when a positive edge occurs on the corresponding Preload input. The value must be between the High and Low Limits or an error will be returned and the command ignored.

Load Oscillator Divider. (1 to 65535)

This command changes the frequency of the square wave oscillator signal. The frequency generated is 1 megahertz (1 MHz) divided by the oscillator divider. Thus to get 50 Hz, the oscillator divider should be 20000.

Chapter 6 Counter Type D

Counter Type D is described in this chapter. The description includes counter operation, configuration of the counter, and the interface between the counter and CPU.

Contents and Operation of a Type D Counter

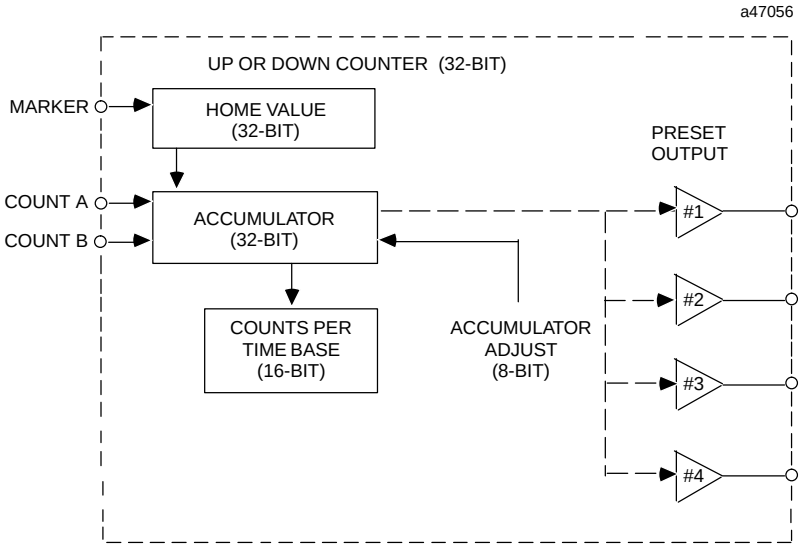
Overview

The Type D counter contains four 32-bit bidirectional counters. Each counter is controlled by 3 of the 12 single ended or differential voltage inputs: Count A, Count B, and Marker. Each counter may be independently configured to count in one of three modes: Up and Down, Pulse with Direction, and A Quad B. Counter Type D elements are shown in the figure below.

Each counter has:

- a 32-bit Accumulator register which counts the pulses from the Count A and Count B inputs
- a Marker input which is used for setting Home Position
- a counts per timebase register which indicates the count rate of the input pulses.

Each of the four 5 to 30 V Preset outputs can be independently assigned to any of the counters, and can be used to generate PLC interrupts.

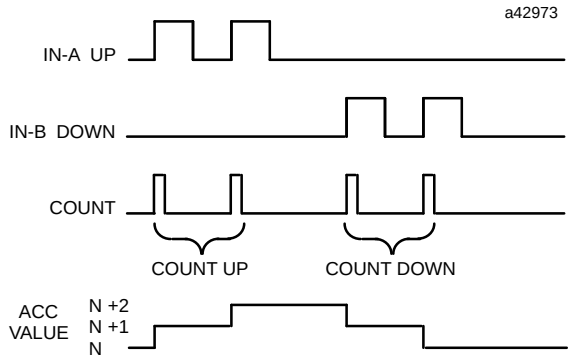


Count A and B Inputs and Accumulator

The 32-bit Accumulator is incremented or decremented based on a configured interpretation of its two count inputs. The interpretation can be set to Up / Down, Pulse / Direction, or A Quad B. Each is Described below.

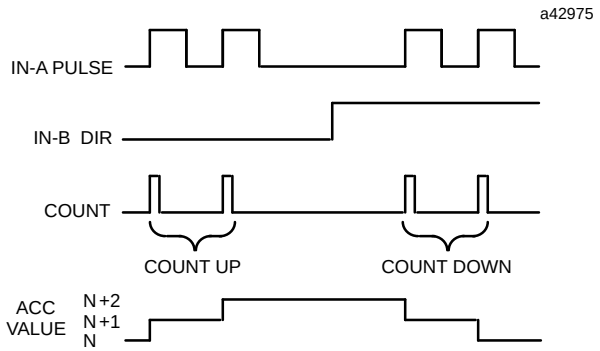
Operating in UP/DOWN Mode

Up-counting occurs on the low-to-high transition of the Up input. Down counting occurs on the low-to-high transition of the Down input. The accumulator automatically tracks the difference between the number of counts received by the Up channel and the Down channel. Simultaneous inputs on the up channel and down channel will cause a net accumulator change of zero.



Operating in Pulse/Direction Mode

Counting always occurs on the low-to-high transition of the Pulse input. Count direction is up for a low level on the Direction input and down for a high level on the Direction input. Avoid changing the DIR signal coincidentally with the rising edge of the Pulse input.



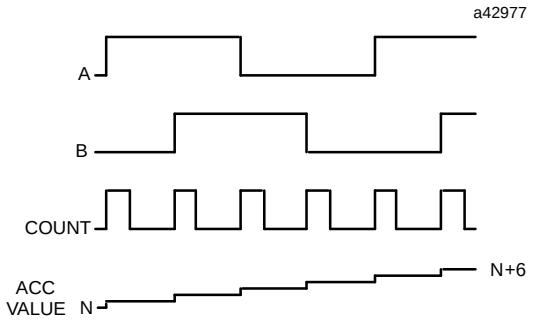
Operating in A Quad B Mode

In A Quad B mode, there are four possible counts for each A Quad B cycle. There are three A Quad B modes which each return a different number of counts per A Quad B cycle. The number of counts per cycle and the count direction is given in the table below:

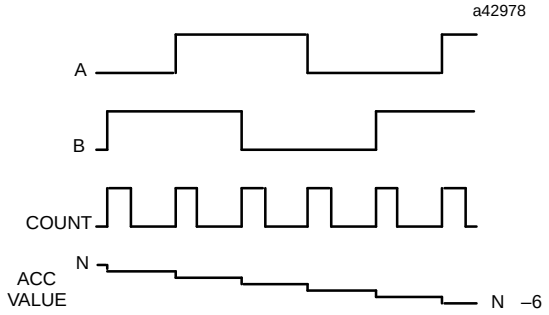
	A Quad B x4	A Quad B x2	A Quad B x1
Counts per Cycle	4	2	1
Up Counts generated when:	A leads B, all edges	A leads B, A edges	A leads B, rising A edge
Down Counts generated when:	B leads A, all edges	B leads A, A edges	B leads A, falling A edge

The counts will be evenly spaced with respect to the input waveforms when the phase relationship between A and B is shifted by 1/4 cycle. The phase relationship between A and B determines count direction. An example of A Quad B x4 counting is shown in the following timing diagrams.

The count direction is up if A leads B.



The count direction is down if A lags B.



Quadrature Error

In any of the A Quad B modes, simultaneous input transitions will generate a quadrature error. When the quadrature error occurs, the counter continues accumulating counts normally until the error is cleared. However, preset outputs assigned to the counter generating the error are set to the configured Output Fail Mode. When the error is cleared, the outputs resume normal operation. The error code indicates which Preset(s) have defaulted due to a quadrature error.

Count Limits

The Accumulator is bounded by a High Limit and a Low Limit. The interaction between the Accumulator and the limits depends on the configured count mode. In Continuous mode, the Accumulator will increment or decrement to the current High or Low Limit, roll over to the other limit, and continue counting. In Single Shot mode, the Accumulator will count to the current High or Low Limit and stop. If the counter direction is changed, the Accumulator will count away from the limit until it reaches the other limit.

The High Limit and Low Limit can be set to any valid 32-bit value at any time using a data command from the PLC. To be a valid 32-bit value, the following conditions must be met: the High Limit must be greater than the Low Limit, the Preload value must be within the High and Low Limit bounds, and any presets pointing to the counter must be within the High and Low Limit bounds. If the limits are changed so the Accumulator is outside the limit boundaries, the Accumulator is set to the Low Limit.

Accumulator

The Accumulator may be set to any 32-bit value within the bounds of the High and Low limits at any time using a data command. Another data command allows the Accumulator to be adjusted by a byte value, from –128 to +127. Finally, a velocity increment can be commanded which causes the Accumulator to increment at a fixed rate.

- the High Limit must be greater than the Low Limit
- the Preload value must be within the High and Low Limit bounds
- the Home value must be within the High and Low Limit bounds
- any presets assigned to the counter must be within the High and Low Limit bounds.

If the limits are changed so the Accumulator is outside the limit boundaries, the Accumulator is set to the Low Limit.

The Accumulator can be set to any 32-bit value within the bounds of the High and Low limits at any time using a data command. Another data command allows the Accumulator to be adjusted by a byte value, from –128 to +127. Finally, a velocity increment can be commanded which causes the Accumulator to increment or decrement at a fixed rate.

Preload Value

On the Type D counter, there is no Preload input. A %Q bit can be sent by the PLC to perform a software preload which sets the accumulator to the Preload Value. The value to which the Accumulator is set when a preload occurs can be configured to any 32-bit value within the range of the high and low limits and has a default value of zero. The Preload value can also be changed using a data command from the PLC.

Marker Input and Home Cycle

The marker input is used to initialize, or home, the counter Accumulator in positioning applications. It can be thought of as an enabled preload. In order to perform a Home Cycle, first the Find Home %Q bit must be set. When the Find Home bit is set, the counter enters the Home Cycle and begins observing the Marker input. On the next

positive Marker transition, the Accumulator is set to the Home Value and a Home Found %I bit is set and returned to the CPU. If the Find Home bit is cleared before a Marker transition is encountered, a Home error is generated and the Home Cycle is aborted. When a Home Cycle is not in progress, the Marker input is ignored.

Counts per Timebase Register

The Counts per Timebase register is a 16-bit register which contains the number of counts received on the Count Pulse input in the last completed timebase interval. It is used to measure the rate of counting. If more counts are received than can be stored in a 16-bit register, the register will overflow. The timebase interval is a configurable value from 1 to 65535 milliseconds.

Changes to the timebase will not take effect until after the previous timebase and one new timebase have elapsed. A Preload will interrupt counting and cause the Counts per Timebase register to be inaccurate for up to two timebase intervals. The timebase is initially configured as 1 second, but may be changed using the Logicmaster 90-70 Configurator function or a data command.

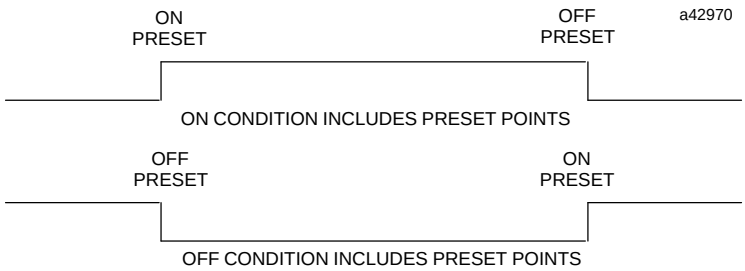
As an unsigned number, the Counts per Timebase register will correctly indicate from 0 to 65536 positive counts received per timebase. As a signed number, it will properly indicate from –32768 to 32767 counts per timebase. The timebase should be selected to not allow more counts in a timebase than the 16-bit register can hold or it will overflow.

Preset Outputs

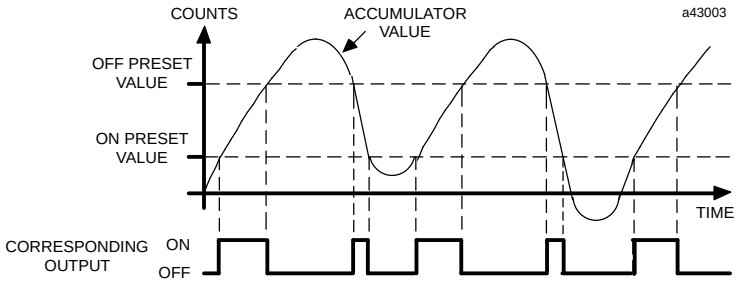
The module has four preset outputs, each of which can be assigned to any counter. Each preset output has a preset ON and preset OFF value, or position, which must be within the count limits of the counter to which the preset is assigned. The preset ON and OFF positions determine when the output will be ON or OFF.

Preset closest to low limit	Output ON	Output OFF
ON	> = ON Preset < = OFF Preset	> OFF Preset < ON Preset
OFF	< OFF Preset > ON Preset	< = ON Preset > = OFF Preset

The output may be either on or off when the accumulator value lies between the Preset points.



For example:



Separation of Preset Points

The count accumulators are compared to the Presets at 0.5 msec intervals. Therefore, to guarantee that the outputs will always switch, the Preset points must be separated by at least the number of counts received in a 0.5 msec time period. For example:

If maximum count rate = 10kHz;
then minimum count separation = (10,000 Hz x .0005 sec) = 5 counts.

Preset Interrupts

Interrupts can be enabled or disabled for each preset output's ON and OFF transition. At the same time a preset output changes state, the CPU is interrupted. %I and %AI data is transferred so that the interrupt routine will see the most current data from the High Speed Counter. Simultaneous preset changes generate only one interrupt to the CPU, so the updated %I data must be used by an interrupt routine to determine which presets changed state and which edge(s) generated the interrupt. Once configured, interrupts can be independently enabled or disabled using data commands. See Appendix B for information on using the interrupt capability.

Output Failure Mode

When the CPU is stopped or lost, counter operation continues normally without interfacing to the CPU. Until the CPU returns or power is cycled, the operation of the Preset outputs can be configured. In Normal mode, the outputs continue to operate as if the CPU were present. Outputs will change state to reflect the counter Accumulators. In Force Off mode, all preset outputs are turned off and remain off until the CPU returns. In Holdlast mode, the preset outputs retain current levels and do not reflect the counter Accumulators. If the CPU returns to operation, the outputs will immediately begin reflecting the counter Accumulators.

The Output Failure mode is applied to preset outputs assigned to an accumulator which experiences a quadrature error. Normal output operation resumes when the quadrature error is cleared by toggling the %Q Clear Error bit.

Oscillator Output

The High Speed Counter module generates a 5V square wave oscillator signal. The oscillator output frequency is determined by the current oscillator divider (set in configuration or by data command) as indicated below:

*Oscillator Frequency (Hz) = 1,000,000 Ï oscillator div*ider

The output frequency ranges from approximately 15 Hz (oscillator divider of 65535) to 1 MHz (oscillator divider of 1).

Table 6-1. Type D Specific Terminal Strip Assignments

Pin	Signal Name	Type D Pin Name	Type D Pin Description
1,3	IN1	COUNTINPUT1A	Counter 1 count A input
2,4	IN2	COUNTINPUT1B	Counter 1 count B input
5,7	IN3	COUNTINPUT2A	Counter 2 count A input
6,8	IN4	COUNTINPUT2B	Counter 2 count B input
11,13	IN5	COUNTER3A	Counter 3 A input
12,14	IN6	COUNTER3B	Counter 3 B input
15,17	IN7	COUNTER4A	Counter 4 A input
16,18	IN8	COUNTER4B	Counter 4 B input
21,23	IN9	MARKER1	Counter 1 marker input
22,24	IN10	MARKER2	Counter 2 marker input
25,27	IN11	MARKER3	Counter 3 marker input
26,28	IN12	MARKER4	Counter 4 marker input

Configuring the Type D High Speed Counter

The following table summarizes all configuration features and default configuration values for the Type D counter.

Configuration Parameter	Description	Values	Defaults
Failure Mde	Output Failure Mode	NORMAL, OFF, HOLD	NORMAL
Osc Divider	Oscillator Divider	1 ... 65535	1000
Count Thrshlds	Count Input Thresholds	NON-TTL, TTL, MAG-PKUP	NON-TTL
Control Thrshlds	Control Input Thresholds	NON-TTL, TTL	NON-TTL
Count Filtr	Count Input Filter	HIFREQ, LOWFREQ	HIFREQ
Preset CTR#	Preset Accumulator	CTR1 ... CTR4	Preset #
Preset ON	Preset ON setpoint	Low Limit ... High Limit	8,388,607
Preset OFF	Preset OFF setpoint	Low Limit ... High Limit	0
ON Interrupt	Preset on transition interrupt	DISABLED, ENABLED	DISABLED
OFF Interrupt	Preset off transition interrupt	DISABLED, ENABLED	DISABLED
Hi Limit	High Count Limit	–2,147,483,648 ... 2,147,483,647	8,388,607
Lo Limit	Low Count Limit	–2,147,483,648 ... 2,147,483,647	0
Count Mode	Count Mode	CONTINU, SINGSHOT	CONTINU
Count Sig	Count Signals	PULSE / DIR, UP / DOWN, A QUAD B X1, A QUAD B X2, A QUAD B X4	PULSE / DIR
Timebase(ms)	Timebase	1 ... 65535 ms	1000 ms
Preld Value	Preload Value	Low Limit ... High Limit	0
Home Value	Home Value	Low Limit ... High Limit	0

Output Failure Mode

When the CPU is stopped or lost, counter operation continues normally; however, the operation of the Preset outputs can be configured until the CPU returns or power is cycled. In all modes, the Accumulators are updated and the Strobes and Preloads are processed normally.

- In Normal mode (NORMAL), the outputs continue to operate as if the CPU were present. Outputs will change state to reflect the counter Accumulators.
- In Force Off mode (OFF), all preset outputs are turned off and remain off until the CPU returns.
- In Holdlast mode (HOLD), the preset outputs retain current levels and do not reflect the counter Accumulators.

If the CPU returns to operation or the module is power-cycled, the outputs will immediately begin reflecting the counter Accumulators again.

The Output Failure mode is applied to preset outputs assigned to an accumulator which experiences a quadrature error. Normal output operation resumes when the quadrature error is cleared by toggling the %Q Clear Error bit.

Oscillator Divider

The oscillator divider is used to generate a 5V oscillator output. The output frequency is 1 million divided by the oscillator divider; the formula is shown below.

Oscillator Frequency (Hz) = 1,000,000 / oscillator divider

The output frequency ranges from approximately 15 Hz (oscillator divider of 65535) to 1 MHz (oscillator divider of 1).

Input Thresholds

All inputs can be used as differential or single-ended inputs. The following table specifies the input thresholds for single-ended and differential use based on threshold selection and input type. The configuration parameters will set input thresholds according to the following table:

Configuration Parameter	Inputs Controlled	Input Definitions
Counter 1 Threshold	IN1, IN2, 1N9, 1N10	Counter 1 Inputs A, B; Marker 1, 2 Inputs
Counter 2 Threshold	IN3, IN4	Counter 2 Inputs A, B
Controller 3 Threshold	IN5, IN6, IN11, IN12	Counter 3 Inputs A, B; Marker 3, 4 Inputs
Controller 4 Threshold	IN7, IN8	Counter 4 Inputs A, B

All of the inputs controlled by a single selection will have the same voltage threshold. The only exception is Marker inputs 1 and 2. If the Counter 1 Threshold is set to Magnetic Pickup, the Marker inputs are set to TTL.

The voltage thresholds which can be selected for each input are described in the following table.

Input Type	Single-Ended			Differential		
	Non-TTL	TTL	Mag-Pickup	Non-TTL	TTL	Mag-Pickup
Counter 1 Threshold	8 V	1.4 V	0.1 V	4.8 V	0.8 V	0.1 V
Counter 2 Threshold	8 V	1.4 V	0.1V	4.8 V	0.8 V	0.1V
Controller 3 Threshold	8 V	1.4 V	X	4.8 V	0.8 V	X
Controller 4 Threshold	8 V	1.4 V	X	4.8 V	0.8 V	X

Input Filters

All inputs default to using a 2.5 microsecond high-frequency filter. The Count inputs for each counter can be configured to use a 12.5 millisecond low-frequency filter instead. The low-frequency filter reduces the effects of signal noise. The Marker inputs always use the high-frequency filter.

Preset Accumulator

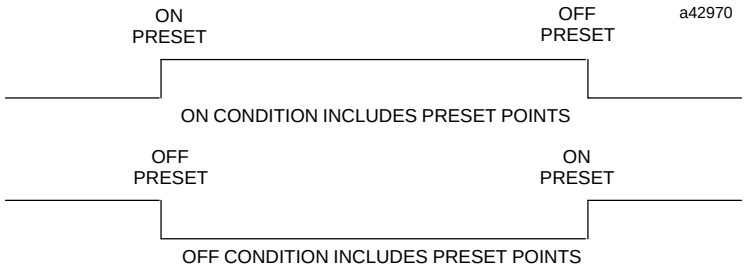
The Preset Accumulator field determines which counter a preset output will reflect. Each of the four preset outputs can be assigned to any of the accumulators. The Preset ON and Preset OFF values must be within the range of the High and Low Limits of the counter the Preset Accumulator is assigned to. The default for each Preset is to reflect the counter of the same number. Thus Preset 1 points to counter 1, Preset 2 points to counter 2, etc.

Output Preset ON and OFF Positions

Each counter output has a preset ON and OFF position. The output state indicates when the counter accumulator value is between the ON and OFF points.

Preset closest to low limit	Output ON	Output OFF
ON	> = ON Preset < = OFF Preset	> OFF Preset < ON Preset
OFF	< OFF Preset > ON Preset	< = ON Preset > = OFF Preset

The output may be either on or off when the accumulator value lies between the Preset points.

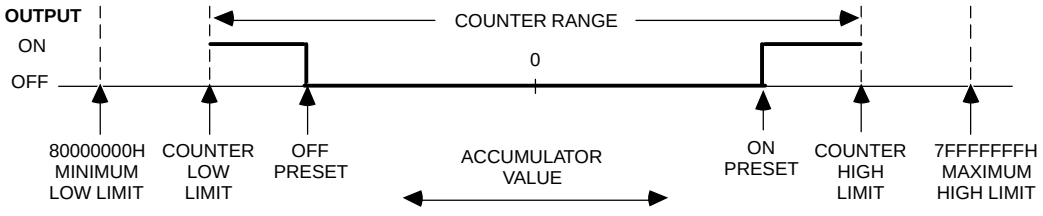


For example:

Location of Preset Points

The Preset points may be located anywhere within the counter range. When the accumulator value is between the Preset points, the output ON / OFF state will always be that of the lowest (most negative) Preset point. When the accumulator value is *not* between the Preset points, the output ON / OFF state will be that of the most positive preset. This is true regardless of the counter direction.

The following example compares the output state and accumulator value of a 32-bit counter when the OFF Preset value is closer to the Low Limit then the ON Preset value.



Preset Interrupt Enables

Each preset can generate an interrupt to the CPU. If the Interrupt ON selection is enabled, then an ON transition of the preset output will generate an interrupt to the CPU. Similarly, if the Interrupt OFF selection is enabled, an OFF transition of the preset output will generate an interrupt to the CPU. Thus no edge, either edge, or both edges of a preset output transition can generate an interrupt. The default is for all interrupts to be disabled.

Count Limits

Each counter is assigned upper and lower count limits. The upper (high) limit must the most positive, and the lower limit must be the most negative. Both limits can be positive or negative, but the high limit must always be greater than the low limit. A counter's Accumulator, Preload value, Home value, and any Preset outputs assigned to the counter must lie within the high and low limits.

If the Accumulator value is outside the new limits when the limits are changed it is automatically adjusted to the low limit value. If the new limits are incompatible, that is, (high < low or low > high), then they will be rejected and the old limits retained. In this case a counter limit error code will be returned. To avoid this situation when the limits are changed one at a time, a good rule to follow is: always move the high limit first when shifting the limits up and always move the low limit first when shifting them down.

As a 32-bit counter, the limit range is –2,147,483,648 to 2,147,483,647.

Count Mode

A counter can be configured to count continuously within the count limits, or to count to a limit and stop.

Continuous Counting

In the continuous counting mode, if either the upper or lower limit is exceeded, the counter wraps around to the other limit and continues counting. Continuous counting is the default mode.

Single-Shot Counting

If single-shot is selected, the counter will count to its upper or lower limit, then stop. When the counter is at the limit, counts in the opposite direction will count it back off the limit. The Accumulator can also be changed by loading a new value from the CPU or by applying a Preset Input.

Count Signal Mode

Each counter can be configured to interpret its Count inputs in one of three ways:

- Up / Down mode mode - rising edges on the A, or up, input increment the Accumulator while positive transitions on the B, or down, input decrement the Accumulator.
- Pulse / Direction mode - rising edges on the A, or pulse, input are counted. If the B, or direction, input is low then the Accumulator is incremented but if the Second input is high then the Accumulator is decremented.
- A Quad B mode - if the A input leads the B input, the Accumulator is incremented and if the B input leads the A input the Accumulator is decremented.

Counter Timebase

For each counter, the timebase represents a span of time which can be used to measure the rate of counting. For example, the program may be required to monitor the number of count pulses which are occurring every 30 seconds.

A timebase from 1 msec to 65535 msec can be selected for each counter. The counter timebase is set to 1 second (1000 msec) by default. The module stores the number of counts that occurred during the last-completed timebase interval in the Counts / Timebase register. The timebase value selected should not allow the Counts / Timebase register to overflow at the maximum count frequency.

The timebase counter updates once each timebase period. After power-up, or any disruption in counting, allow at least one timebase period for the counter to stabilize.

Preload Value

For each counter, a starting, or Preload, value can be specified which will be used when the Preload input is activated. This Preload value is used for both hardware and software preloads. If the counter should be reset to zero, enter 0 as the Preload value; this is the default value. The preload range is –2,147,483,648 to +2,147,483,647, but it must be within the counter limits.

Data Transfer Between High Speed Counter and CPU

The Series 90-70 High Speed Counter updates the %I and %AI data every 0.5 milliseconds. The Series 90-70 CPU reads this data immediately preceding every pass through the ladder logic, before triggering a ladder interrupt, and when a DOIO specifically requesting this data is performed in the ladder logic. To support the unique data coherency requirements of the High Speed Counter, the CPU reads both the %I and %AI data when performing DOIOs requesting only %I data.

The format of this input data depends on whether the counter is configured as Type A, Type B, Type C, or Type D. In return, during each I/O scan, the CPU sends 32 bits (%Q) of control data and 6 words (%AQ) of output data commands to the module. COMMREQ function blocks in the user program can also be used to send additional data commands to the module.

See Appendix A for more information about the COMMREQ and DOIO functions.

%I and %AI Data Sent by a Module Configured as Type D

The 32 status bits (%I) represent:

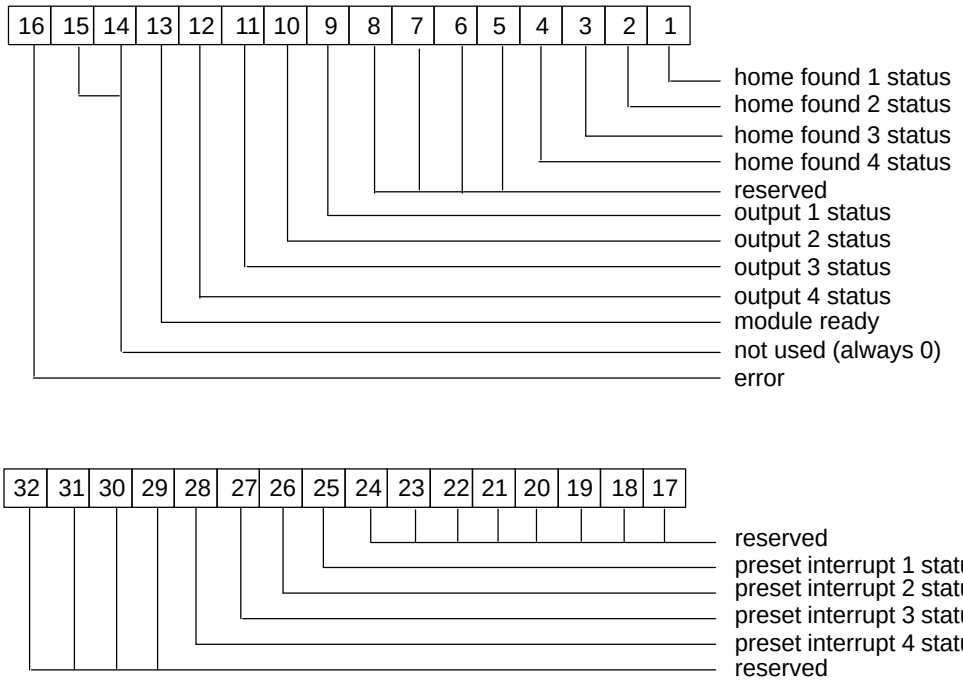
- Home Found flag
- Output status
- Module ready status
- Error status
- Interrupt status

These status bits are sent to the CPU as inputs, and can influence outputs sent from the CPU to the module.

The 16 register data words (%AI) represent:

- Module Status Code
- Counts per Timebase value
- Accumulators

Status Bits (%I) - Type D Counter



Home Found

This bit indicates the completion of the Home Cycle. It is set on the rising edge of the Marker input when the Find Home %Q bit is set. When the Find Home %Q bit is cleared and then set again, the Home Found bit is cleared.

Output Status

These bits indicate the ON or OFF state of the four preset outputs.

Module Ready

This bit is set after the module completes its power-up tests.

Error Status

This bit is set when an error occurs. If it is set, a module status code has been returned in the first %AI location and the board OK LED flashes at 4 Hz. The Error Status bit is cleared by setting the Clear Error %Q bit.

Preset Interrupt Status

These bits are set by the High Speed Counter when the corresponding preset output has changed state and generated an interrupt. These flags can be used by an interrupt routine to determine which outputs have generated interrupts. The Output Status bits can be used in conjunction with the Preset Interrupt Status bits to determine which transition caused the interrupt. The Preset Interrupt Status bits should only be tested in a ladder logic interrupt handler.

%AI Data - Type D Counter

Word	Description	Word	Description
01	Module Status code	06 - 07	Accumulator for counter 1
02	Counts per timebase for counter 1	08 - 09	Accumulator for counter 2
03	Counts per timebase for counter 2	10 - 11	Accumulator for counter 3
04	Counts per timebase for counter 3	12 - 13	Accumulator for counter 4
05	Counts per timebase for counter 4	14 - 16	Not used (set to 0)

Module Status Codes

The Module Status Code in the %AI Input Data contains the error code returned to the PLC. The HSC sets this code to indicate a data command or configuration error. For all error codes except quadrature errors, once an error code has been returned, no more errors will be generated until the error is cleared. Quadrature errors are unlike other errors in that they are cumulative and the Counter Number will be updated to indicate additional quadrature errors. To clear a module status code, eliminate the condition that caused the error, and toggle the Clear Error %Q bit.

Note that fatal errors (RAM, EPROM) have no codes associated with them because these errors cause the watchdog timer to time out and the board to go into constant reset.

The error code format is given below, followed by a list of error codes on the following page.

High Byte		Low Byte
Error Source	Counter or Preset #	Error Code

Error Codes for Type D

Error Code	Error Type	Definition
00	No Error	No Error Present
03	Command Errors	Home Error
04		Quadrature Error
11		Unknown Command
21		Invalid Counter or Preset
31		Invalid COMMREQ task ID
41		Velocity Increment Out of Range
81		Accumulator Out of Range
91		Preload Value Out of Range
B1		Home Value Out of range
C1		Preset ON Out of Range
D1		Preset OFF Out of Range
12	Limit Errors	High Limit < Low Limit
22		Range Excludes Preload
52		Range Excludes Preset ON
62		Range Excludes Preset OFF

Error Codes for Type D (continued)

18	Configuration Errors	High Limit < Low Limit
28		Range Excludes Preload Value
48		Range Excludes Home Value
58		Range Excludes Preset ON
68		Range Excludes Preset OFF
A8		Unsupported Feature Error
B8		Unknown Counter Type
C8		PLC Version Error
D8		Logicmaster 90 Version Error

Configuration Errors are not returned in %AI data since the module does not configure, but the error code is returned in the IO Fault data.

Counter or Preset Number

For a valid command (recognized value in byte 0), the counter or preset number, from 1 to 4, that generated the error will be reported. A preset number only appears in error codes C1 and D1.

In the case of the Home and Quadrature Errors, multiple errors could occur at the same time. Thus each bit represents a counter and the value is the logical OR of these bits. The following table shows the value for each counter.

Value	Counter #
1	1
2	2
4	3
8	4

Thus, a value of 9h (hexadecimal), with the error code 04 would mean both counter 1 and counter 4 had Home Errors occur at the same time.

Error Source

Command and Limit errors return the source of the error.

Value	Error Source
1	%AQ Command 1 (%AQ Offset 0-2)
2	%AQ Command 2 (%AQ Offset 3-5)
4	COMMREQ Function

Example:

If the hexadecimal data 0002 0000 0107 was placed into the %AQ offsets 3 through 5, the error 2141h (hexadecimal) would be reported. The module status code represents:

Value	Representation
2	Error in %AQ Command 2
1	Error generated by counter 1
41	Velocity Increment Out of Range

%Q and %AQ Data Sent from CPU to HSC Configured as Type D

Once each I/O scan, the CPU sends eight words of data (32 bits of %Q and six words of %AQ) to the High Speed Counter Module. The application program can use these outputs to control the module.

The 32 output bits (%Q) represent:

- Home Command
- Clear error flag
- Output enable
- Preload Accumulator

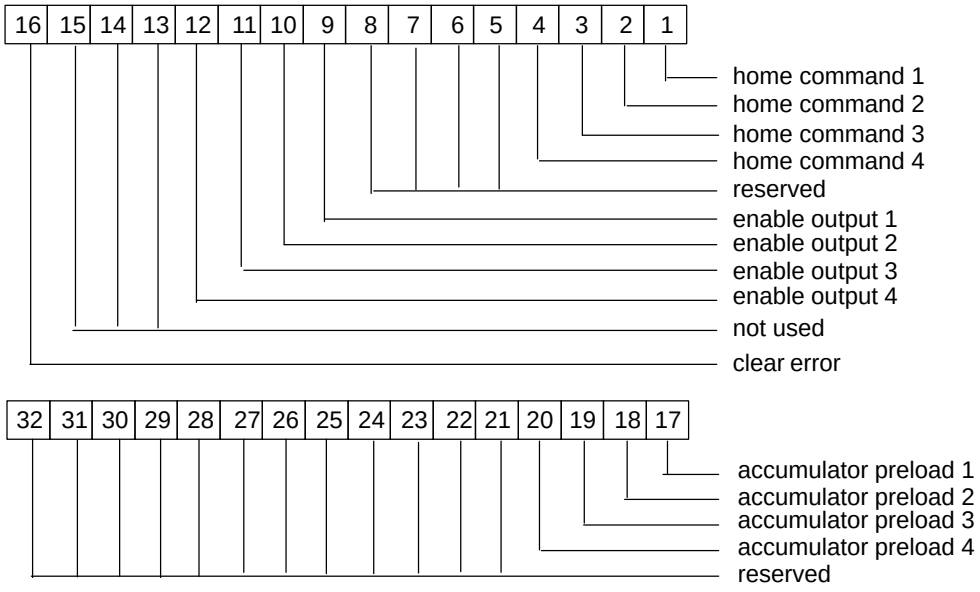
Six Words (%AQ) of Command Data

The 6 words of command data, which can also be sent using a COMMREQ Function Block, can perform the following operations:

- Load Accumulator
- Load count limits
- Load Accumulator increment
- Load output preset values
- Load Preload value
- Load time base
- Load Oscillator divider
- Set Count Direction
- Enable/Disableinterrupts
- Load Home value

All of this data is transferred from the High Speed Counter to the CPU once per I/O scan. The I/O scan is active while the CPU is in the RUN mode or STOP ENABLED mode.

%Q Data



Home Command

This bit is used to start a Home Cycle. When this bit transitions ON, the Marker input is monitored. When a rising edge occurs on the Marker input, the Accumulator is set to the Home value and the Home Found %I bit is set. If the Home Command bit is cleared before a Marker transition is encountered, a Home Error occurs.

Enable Output

These bits enable the corresponding preset output. If cleared, the output will always be OFF and not reflect the accumulator's value in relation to the Preset ON and OFF values.

Clear Error

This bit should be set by the CPU to clear the Error Status %I bit after the error has been acknowledged. This bit is rising edge active, so new errors may appear while set.

Preload Accumulator

These bits tell the counter to perform a software preload and set the corresponding Accumulator to the Preload value. They do NOT, however, cause the corresponding Preload Status bit to be set.

Data Commands for Counter Type D

At the end of every CPU sweep, six words of %AQ data are automatically transferred from the CPU to the High Speed Counter. These six words are used to send data commands from the PLC to the HSC. The first three words, offsets 0 through 2, make up %AQ command 1, and the second three words, offsets 3 through 5, make up a completely separate %AQ command 2. Thus two commands can be sent to the HSC at the end of each sweep. Note that %AQ command 1 is executed first, so that if identical commands with different values are sent to the HSC simultaneously, %AQ command 2 data will overwrite %AQ command 1 data.

Even though the %AQ data is sent each sweep, commands are acted on ONLY if the command has changed since the last sweep. When any of the 6 bytes in a command changes, the HSC will accept the data as a new command and respond accordingly.

The DOIO function is supported, so that data can be transferred between the CPU and HSC mid-sweep. Note that to ensure that the High Speed Counter has time to process DOIO data sent to it, the application should not change the data more frequently than every 0.5 millisecond. Because data sent to the HSC is updated at the end of the CPU sweep, half a millisecond should elapse between the beginning of the sweep and a DOIO function block, between two DOIO function blocks, and between a DOIO function block and the end of the sweep.

The COMMREQ function block can also be used to send data commands to the HSC mid-sweep. COMMREQs must be separated only from each other, and by at least 0.5 milliseconds. A description and example of the use of COMMREQs and DOIOs is given in Appendix A.

%Q data is processed by the HSC before the %AQ data. Therefore commands that can be affected by %Q bit operations should be sent at least one sweep before the %Q bit operation. For example, the Load Preload Value command should be sent one sweep before setting the Preload Accumulator %Q bit to preload that value.

In describing data commands, word offsets are shown in reverse order and in hexadecimal to simplify data entry. The following example sends a Load Accumulator Counts command with value 0001 to counter 2 using offsets 0 through 2.

The first word, or command word, which goes into word offset 0 would be 0201h. The value 01 in byte 0 represents the command Load Accumulator Value. The value 02 in byte 1 is the counter number, in this case counter 2. For the Load Accumulator Value command, word 1 is the sixteen bit value to be loaded into the accumulator and word 2 is ignored. In this example, word 1 would have the value 0001h because that is the value to be placed in the accumulator. Word 2 will be ignored and can be anything, but it is usually best to use the value 0. If word offset 0 corresponded to %AQ1, the complete command to load the counter 2 accumulator with value 0001 would be:

%AQ3 (word 2)	%AQ2 (word 1)	%AQ1 (word 0)
0000	0001	0201

The following table is a list of data commands for counter Type D. Byte 0 data is given in hexadecimal.

Command Definition	Data				Command Word	
	Word 2		Word 1		Word 0	
	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
Null	xx	xx	xx	xx	xx	00h
Load Accumulator Value	data (32)				n	01h
Load High Limit	data (32)				n	02h
Load Low Limit	data (32)				n	03h
Load Accumulator Increment	xx	xx	xx	data (8)	n	04h
Load Timebase	xx	xx	data (16)		n	06h
Load Velocity	xx	data (24)			n	07h
Load Home Value	data (32)				m	0Bh
Load Preset ON Value	data (32)				m	0Bh
Enable/Disable Preset ON Interrupt	xx	xx	xx	data (8)	m	0Fh
Load Preset OFF Value	data (32)				m	15h
Enable/Disable Preset OFF Interrupt	xx	xx	xx	data (8)	m	19h
Load Preload Value	data (32)				n	1Fh
Load Oscillator Divider	xx	xx	data (16)		0	32h

m = Preset Number (1 to 4); n = Counter Number (1 or 2);

xx = Do not care (ignored); data (8, 16, 24, 32) = 8, 16, 24, or 32 bit data

Descriptions of each command are given below. The valid range of values is given in parenthesis.

Null

This is the default %AQ data command. Since the %AQ data is transferred each PLC sweep, it is a good idea to have the Null command present when not executing a specific data command to avoid inadvertent execution. All data is ignored with a Null command.

Load Accumulator Value (Low Limit to High Limit)

This command places a 32-bit value into a counter accumulator. The value must be within the Count Limits, or an error will be returned and the command ignored.

Load High Limit (–2,147,483,648 to 2,147,483,647)

This command sets the highest value to which a counter will count. Counts that would cause the counter to go higher are ignored or cause the accumulator to roll over to the Low Limit depending on whether the counter is configured for Single-shot or Continuous count mode. The High Limit can be any 32-bit value with the following restrictions: it must be greater than the Low Limit, the counter's Preload value must lie between it and the Low Limit, and all preset outputs which are assigned to the counter must have preset ON and OFF values which lie between it and the Low Limit. If a restriction is not met, an error will be generated and the command ignored. If the range between the Low Limit and the new High Limit excludes the Accumulator, the Accumulator will be set to the Low Limit and no error is generated.

Load Low Limit (–2,147,483,648 to 2,147,483,6477)

This command sets the lowest value to which a counter will count. Counts that would cause the counter to go lower are ignored or cause the accumulator to roll over to the High Limit depending on whether the counter is configured for Single-shot or Continuous count mode. The Low Limit can be any 32-bit value with the following restrictions: it must be less than the High Limit, the counter's Preload value must lie between it and the High Limit, and all preset outputs which are assigned to the counter must have preset ON and OFF values which lie between it and the High Limit. If a restriction is not met, an error will be generated and the command ignored. If the range between the new Low Limit and the High Limit excludes the Accumulator, the Accumulator will be set to the Low Limit and no error is generated.

Load Accumulator Increment (–128 to 127 counts)

The Accumulator Increment performs a one-shot adjustment to the accumulator. Only byte 2 is used for data, all other data bytes are ignored. The one-shot increment may be performed at any time, even when counting at maximum rate. If the offset cause the counter to exceed its limits, the excess is treated just like any other overflow, i.e., in Continuous mode the Accumulator rolls over to the other limit and in Single-shot mode the Accumulator does not pass the limit.

Load Timebase (1 to 65535 milliseconds)

This command sets the timebase. The timebase is the number of milliseconds for which the counter counts input pulses and then returns in the Counts per Timebase register. If the timebase is 1000, or 1 second, the Counts per Timebase register returns the number of counts detected in each 1 second period. Any non-zero 16-bit value may be used as the timebase.

Load Velocity (–100,000 to 100,000 counts per second)

A velocity increment is an internal count generator, or a continuous accumulator increment. Each millisecond, 0.1% of the increment value is added to the accumulator. A value of 0 will stop the velocity increment. Counts from the velocity increment are cumulative with counts coming in from the Count Pulse input. Note that counts generated by the velocity increment are not reflected in the Counts per Timebase register.

Load Home Value (Low Limit to High Limit)

The Load Home command sets the value to which the Accumulator will be set when a positive edge occurs on the Marker input while in a Home Cycle. The value must be between the High and Low Limits or an error will be returned and the command ignored.

Load ON and OFF Preset Value (Count Limits of the assigned counter)

This command sets the preset output turn on and turn off points within a counters range. Preset values can be any value between the high and low limits.

Enable/Disable Preset ON and OFF Interrupts (0=Disable, 1=Enable)

This command enables or disables interrupts resulting from Preset output transitions. For example, if Preset ON interrupts are enabled, then a low to high transition of the Preset ON output will generate an interrupt to the CPU. This command allows the interrupts to be enabled or disabled within a ladder.

Load Preload Value (Low Limit to High Limit)

The Load Preload command sets the value to which the Accumulator will be set when a positive edge occurs on the Preload input. The value must be between the High and Low Limits or an error will be returned and the command ignored.

Load Oscillator Divider (1 to 65535)

This command changes the frequency of the square wave oscillator signal. The frequency generated is 1 megahertz (1 MHz) divided by the oscillator divider. Thus to get 50 Hz, the oscillator divider should be 20000.

Chapter 7 Counter Type E

Counter Type E is described in this chapter. The description includes counter operation, configuration of the counter, and the interface between the counter and CPU.

Contents and Operation of a Type E Counter

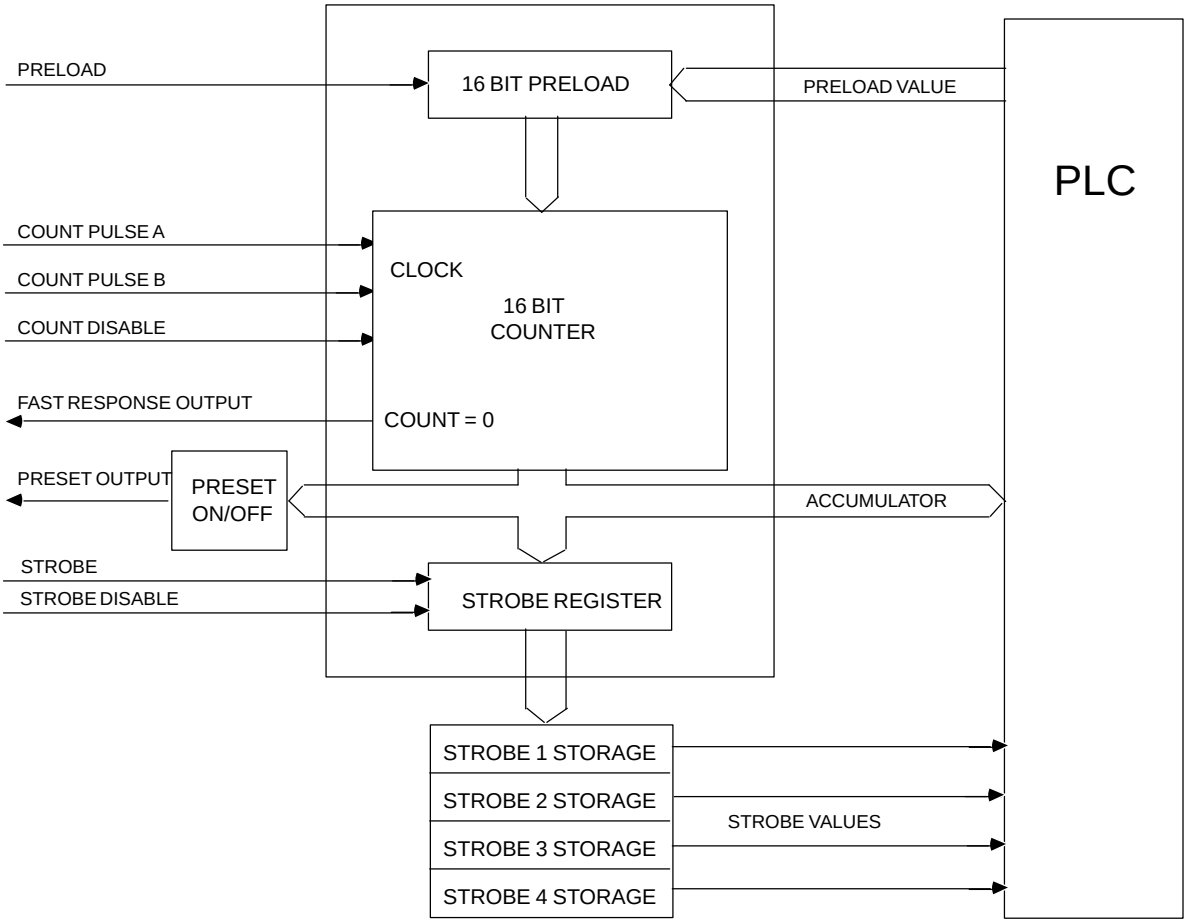
Overview

The Type E counter contains two 16-bit bidirectional counters, each of which has a single, dedicated fast response preset output. Each counter is controlled by 6 of the 12 single ended or differential voltage inputs: Count A, Count B, Strobe, Strobe Disable, Count Disable, and Preload. Each counter can be independently configured to count in one of two modes: Up and Down or A Quad B. The Type E counter supports a maximum count rate of 200 KHz in Up / Down mode, and 800 KHz in A Quad B mode. Counter Type E elements are shown in the illustration on the following page.

Each counter has:

- a 16-bit Accumulator register which counts the pulses from the Count A and Count B inputs
- a Fast Preset Output, which will turn on within 10 µS of the Accumulator counting down to zero
- a Disable input which causes the Accumulator to ignore count pulses.
- Four Strobe registers which store the Accumulator value when a Strobe input transitions
- a Strobe Disable that causes the counter to ignore strobe pulses
- a preload value which is inserted into the Accumulator when a preload occurs

In addition to the two Fast Preset Outputs, there are two standard preset outputs that can be assigned to either accumulator, and have configurable on and off limits.

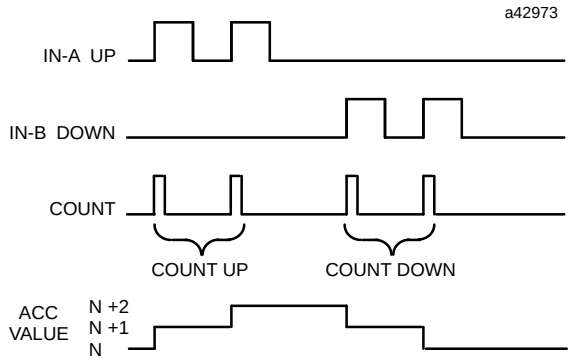


Count A and B Inputs and Accumulator

The 16-bit Accumulator is incremented or decremented based on a configured interpretation of its two count inputs. The interpretation can be set to Up / Down or A Quad B. Each is described below.

Operating in UP/DOWN Mode

Up-counting occurs on the low-to-high transition of the Up input. Down counting occurs on the low-to-high transition of the Down input. The accumulator automatically tracks the difference between the number of counts received by the Up channel and the Down channel. Simultaneous inputs on the up channel and down channel will cause a net accumulator change of zero.

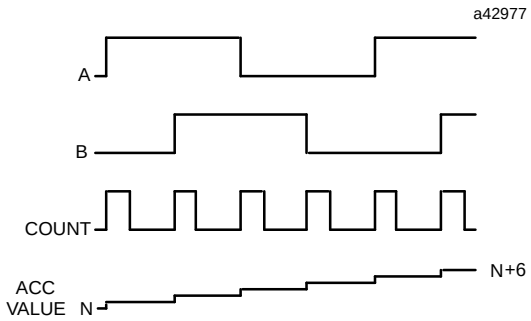


Operating in A Quad B Mode

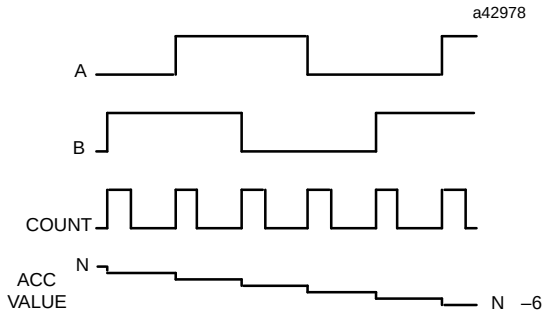
In A Quad B mode, there are four counts for each A Quad B cycle. A count occurs for each transition of either A or B. The counts will be evenly spaced with respect to the input waveforms when the phase relationship between A and B is shifted by 1/4 cycle.

The phase relationship between A and B determines count direction, as shown in the following timing diagrams.

The count direction is up if A leads B.



The count direction is down if A lags B.



The Type E is designed primarily as a down counter, operating between the configured Preload value and zero. When the Accumulator counts down to zero, the associated Fast Preset Output will turn on. If configured for Continuous counting, the Accumulator will automatically Preload itself when the Accumulator decrements to 0 and continue

counting. If configured for Single Shot operation, the Accumulator will count down to zero and stay there until it receives a Preload. Although primarily designed for down-counting, up counting is supported to accommodate momentary up counts (such as *jitter* on an A Quad B input). The preset output is not energized if the counter counts up from 65,535 and rolls over to 0.

In the Type E counter, the count limits are effectively defined by the Preload value and zero. The Preload value can be set to any unsigned 16-bit value at any time using a data command from the PLC. The new Preload value will not affect counting until the counter is preloaded or decrements to zero in continuous mode.

At power-up the accumulators are initialized to the configured preload value.

Strobe Inputs and the Strobe Event Stack

Each Strobe input is an edge sensitive input which can be configured to respond to a positive edge, negative edge, or both positive and negative edges. Each counter has a four register Strobe Event Stack. When the configured Strobe input transition occurs, called a Strobe Pulse, the value in the Accumulator is stored in the first available register in the Strobe Stack, and the corresponding strobe flag is set and returned in %I data to indicate the event to the CPU. Subsequent strobes are captured and reported in a similar manner until the stack is full. The CPU acknowledges strobes by toggling the Reset Strobes %Q bit, which resets all the strobe bits and enables four more strobes. The minimum interval between successive strobes is .5 milliseconds.

Preloading the accumulator will automatically reset the Strobe Stack. If the counter is configured for Continuous counting, the strobe stack will automatically be reset and all four strobe flags cleared when the counter decrements to 0 and performs the automatic preload.

If a Strobe occurs within .5 milliseconds of a preload, the strobed value will be stored in the first available Strobe Stack entry, however it is possible that the strobe status will be reset before the strobe status %Q bit has been transferred to the CPU.

Preload Input and Value

Each counter has a 16-bit preload register which is used to initialize the counter when a preload input is detected, when the PLC %Q preload bit has been set, or when the counter decrements to zero in continuous mode. The value to which the Accumulator is set when a preload occurs can be configured to any non-zero unsigned 16-bit value, and has a default value of 1000. The Preload value can also be changed using a data command from the PLC. The Preload input is positive edge sensitive only. Likewise, the %Q preload bit will only cause a preload when the bit transitions from an off to an on state. The preload flag is set and returned in %I data any time that the counter decrements to zero in continuous mode or a positive transition occurs on the Preload input. If an application program uses this flag indication, it should use the corresponding %Q bit to clear the preload flag before the next preload occurs. **A rising edge on the Preload input or a %Q off-to-on transition always preloads the Accumulator regardless of the state of the Preload flag.**

Preset Outputs (Fast Response)

Each counter has one fast response output that turns on within 15 microseconds of the counter decrementing to 0. A PLC interrupt can be enabled to occur for each On transition. In addition, each counter module supports two standard response (0.5 millisecond) outputs which can be assigned to either counter.

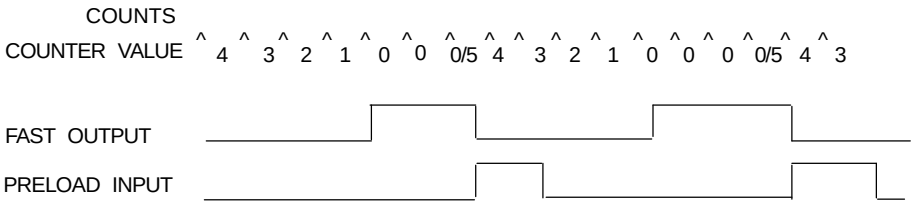
Output operation in Single Shot Counter Mode

The output will have two configuration modes, **Latched** and **Pulse**.

In the Latched mode, the preset output turns on when the counter counts to 0 and remains on until a Preload occurs. A Preload will turn the output off and it will remain off until the counter counts to 0 as illustrated below:

Counter Mode = **Single Shot**

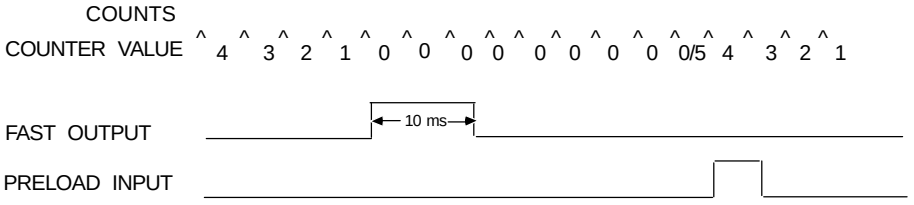
Output Mode = **Latched** Preload Value = 5



In the **Pulse** mode the preset output turns on when the counter counts to 0, and remains on for a duration configured by the user. The configured pulse duration can be 1 millisecond to 1 second with 1 millisecond resolution. Operation in this mode is illustrated below:

Counter Mode = **Single Shot** Preload Value = 5

Output Mode = **Pulsed** Pulse Length = 10 ms

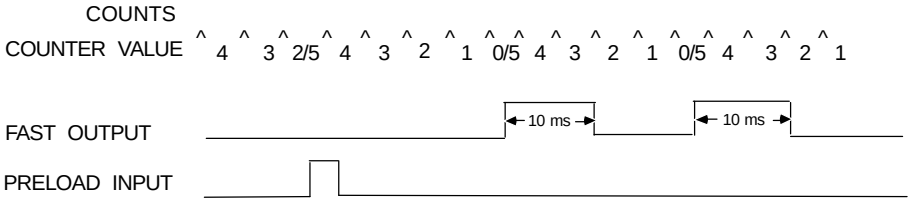


Output operation in Continuous Counter Mode

In Continuous Mode, only the output pulse mode is applicable . When the counter counts down to 0, the output will pulse on for the configured pulse length time. Operation in the Continuous Mode is illustrated below:

Counter Mode = **Continuous** Preload Value = 5

Output Mode = **Pulsed** Pulse Length = 10 ms



Note

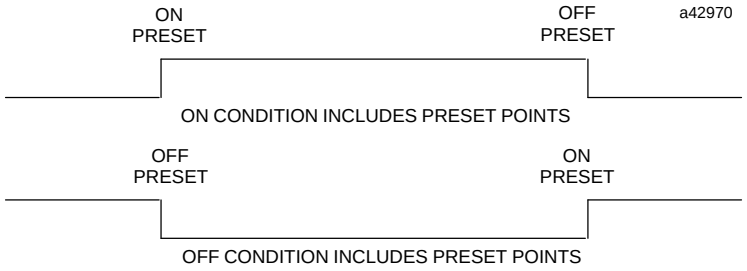
When configured for continuous counting with pulsed outputs, the configured pulse duration must be at least .75 milliseconds less than the time required to count from the preload down to zero. This is to ensure that the pulse has had time to turn off before it is set again.

Preset Outputs (Standard)

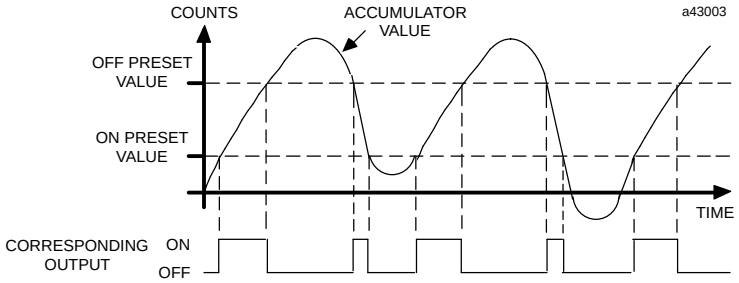
The module has two standard preset outputs, each of which can be assigned to either counter or disabled. When enabled, each preset output has a 16-bit preset ON and preset OFF value. The preset ON and OFF positions determine when the output will be ON or OFF as shown below.

Preset closest to Zero	Output ON	Output OFF
ON	> = ON Preset < = OFF Preset	> OFF Preset < ON Preset
OFF	< OFF Preset > ON Preset	< = ON Preset > = OFF Preset

The output may be either on or off when the accumulator value lies between the Preset points.



For example:



Separation of Preset Points

The count accumulators are compared to the Presets at 0.5 millisecond intervals. Therefore, to guarantee that the outputs will always switch, the Preset points must be separated by at least the number of counts received in a 0.5 millisecond time period. For example:

If maximum count rate = 10KHz;
then minimum count separation = (10,000 Hz x .0005 sec) = 5 counts.

Preset Interrupts

The Fast Preset Outputs support preset ON transition interrupts only. The Standard Preset Outputs interrupts can be enabled or disabled for each preset output's ON and

OFF transition. At the same time a preset output changes state the CPU is interrupted and the corresponding %I and %AI data is automatically transferred so that an interrupt routine will see the current data from the High Speed Counter. The interrupt handler routine can determine which preset transition occurred and which edge generated the interrupt by examining the %I data. Simultaneous transitions on multiple presets will generate a single interrupt to the CPU. Interrupt enables are configurable, with the default being disabled, and can be changed via data commands. See Appendix B for information on using the interrupt capability.

Output Failure Mode

When the CPU is stopped or lost, counter operation continues normally without interfacing to the CPU. The operation of the Preset outputs until the CPU returns to run mode or power is cycled can be configured. In Normal mode, the outputs continue to operate as if the CPU were present. Outputs will change state to reflect the count Accumulators. In Force Off mode, all preset outputs are turned off and remain off until the CPU returns. In Holdlast mode, the preset outputs retain current levels and do not reflect the counter Accumulators. If the CPU returns to operation, the outputs will immediately resume reflecting the counter Accumulators.

Oscillator Output

The High Speed Counter module generates a 5V square wave oscillator signal. The oscillator output frequency is determined by the current oscillator divider (set in configuration or by data command) as indicated below:

Oscillator Frequency (Hz) = 1,000,000 Ï oscillator divider

The output frequency ranges from approximately 15 Hz (oscillator divider of 65535) to 1 MHz (oscillator divider of 1).

Table 7-1. Type E Specific Terminal Strip Assignments

Pin	Signal Name	Type E Pin Name	Type E Pin Description
1,3	IN1	COUNTINPUT1A	Counter 1 count A input
2,4	IN2	COUNTINPUT1B	Counter 1 count B input
5,7	IN3	COUNTINPUT2A	Counter 2 count A input
6,8	IN4	COUNTINPUT2B	Counter 2 count B input
11,13	IN5	CTR1 PRELOAD	Counter 1 preload input
12,14	IN6	CTR1 DISABLE	Counter 1 disable input
15,17	IN7	CTR2 PRELOAD	Counter 2 preload input
16,18	IN8	CTR2 DISABLE	Counter 2 disable input
21,23	IN9	CTR1 STROBE	Counter 1 strobe 1 input
22,24	IN10	CTR1 STROBE DISABLE	Counter 1 strobe disable input
25,27	IN11	CTR2 STROBE	Counter 2 strobe input
26,28	IN12	CTR2 STROBE DISABLE	Counter 2 strobe disable input

Configuring the Type E High Speed Counter

The following table summarizes all configuration features and default configuration values for the Type E counter.

Configuration Parameter	Description	Values	Default
Failure Mde	Output Failure Mode	NORMAL, OFF, HOLD	NORMAL
Osc Divider	Oscillator Divider	1 ... 65535	1000
Count Thrshlds	Count Input Thresholds	NON-TTL, TTL, MAG-PKUP	NON-TTL
Control Thrshlds	Control Input Thresholds	NON-TTL, TTL	NON-TTL
Count Filtr	Count Input Filter	HIFREQ, LOWFREQ	HIFREQ
Preld Filtr	Preload Input Filter	HIFREQ, LOWFREQ	HIFREQ
Cnt Disbl Filtr	Disable Input Filter	HIFREQ, LOWFREQ	HIFREQ
Output Mode	Fast Preset Outpurt Mode	LATCHED, PULSE	PULSE
Outpulse ms	Fast Preset Output Pulse Duration (Pulse Mode Only)	1 ... 1000	10
* Preset CTR#	Preset Accumulator	CTR1, CTR2, DISABLE	** St. Preset #
* On	Preset ON setpoint	Low Limit ... High Limit	65535
* Off	Preset OFF setpoint	Low Limit ... High Limit	0
Interrupt ON	Preset on transition interrupt	DISABLED, ENABLED	DISABLED
* Interrupt OFF	Preset off transition interrupt	DISABLED, ENABLED	DISABLED
Count Mode	Count Mode	CONTINU, SINGSHOT	CONTINU
Count Sig	Count Signals	UP, DOWN, A QUAD B	UP / DOWN
Preld Value	Preload Value	0 ... 65535	1000
Strobe Edge	Strobe Edge	POS, NEG, BOTH	POS

* These items apply to the standard preset outputs (outputs 3 and 4) only.
** Counter 1 is the default counter for output 3, counter 2 is the default counter for output 4.

Output Failure Mode

When the CPU is stopped or lost, counter operation continues normally without interfacing to the CPU. Until the CPU returns or power is cycled, the operation of the Preset outputs can be configured. In all modes, the Accumulators are updated and the Strobes and Preloads are processed.

- In Normal mode (NORMAL), the outputs continue to operate as if the CPU were present. Outputs will change state to reflect the counter Accumulators.
- In Force Off mode (OFF), all preset outputs are turned off and remain off until the CPU returns.
- In Holdlast mode (HOLD), the preset outputs retain current levels and do not reflect the counter Accumulators.

If the CPU returns to operation or the module is power-cycled, the outputs will immediately begin reflecting the counter Accumulators again.

Oscillator Divider

The oscillator divider is used to generate a 5V oscillator output. The output frequency is 1 million divided by the oscillator divider; the formula is shown below.

Oscillator Frequency (Hz) = 1,000,000 Ï oscillator divider

The output frequency ranges from approximately 15 Hz (oscillator divider of 65535) to 1 MHz (oscillator divider of 1).

Input Thresholds

All inputs can be used as differential or single-ended inputs. The following table specifies the input thresholds for single-ended and differential use based on threshold selection and input type. Non-TTL is the default for all inputs.

Configuration Parameter	Inputs Controlled	Input Definitions
Count Threshold 1	IN1, IN2	Counter 1, Inputs A, B
Count Threshold 2	IN3, IN4	Counter 2, Inputs A, B
Control Threshold 1	IN5, IN6, IN9, IN10	Ctr 1 Preload, Count Disable, Strobe, Strobe Disable
Control Threshold 2	IN7, IN8, IN11, IN12	Ctr 2 Preload, Count Disable, Strobe, Strobe Disable

Note that all the inputs controlled will have the same voltage threshold.

The voltage thresholds which can be selected for each input are described in the following table.

Input Type	Single-Ended			Differential		
	Non-TTL	TTL	Mag-Pickup	Non-TTL	TTL	Mag-Pickup
Count Threshold 1	8 V	1.4 V	0.1 V	4.8 V	0.8 V	0.1 V
Count Threshold 2	8 V	1.4 V	0.1V	4.8 V	0.8 V	0.1V
Control Threshold 1	8 V	1.4 V	X	4.8 V	0.8 V	X
Control Threshold 2	8 V	1.4 V	X	4.8 V	0.8 V	X

Only the Count inputs can be configured for Magnetic Pickup thresholds.

Input Filters

All inputs default to using a 2.5 microsecond high-frequency filter. Each Count, Preload, and Disable input can be configured to use a 12.5 millisecond low-frequency filter instead. The low-frequency filter reduces the effects of signal noise. The Strobe inputs always use the high-frequency filter.

Output Mode

The Fast Preset Outputs can be configured for two modes of operation. In Pulse mode, the presets will turn on when the counter decrements to zero, and stay on for the duration configured by the Outpulse mS parameter. In Latched mode, the preset will remain on until the counter is preloaded using either a software or terminal strip preload.

Outpulse Milliseconds

When a Fast Preset Output mode is configured in pulse mode, this parameter is used to program the duration that the output will remain on.

Note

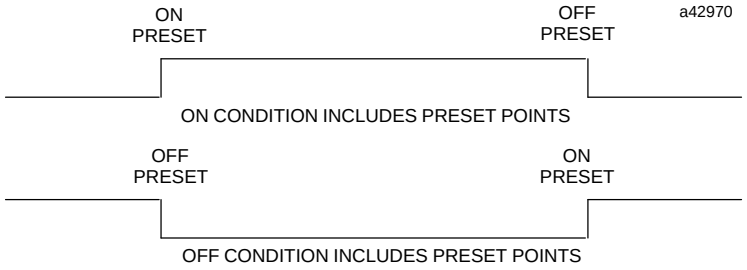
When configured for continuous counting with pulsed outputs, the configured pulse duration must be at least .75 milliseconds less than the time required to count from the preload down to zero. This is to ensure that the output has had time to turn off before being set again.

Preset Accumulator

The Preset Accumulator field determines which counter a preset output will reflect. The two standard preset outputs can be configured to reference to either . The default configuration references Preset 3 to counter 1, and Preset 4 to counter 2.

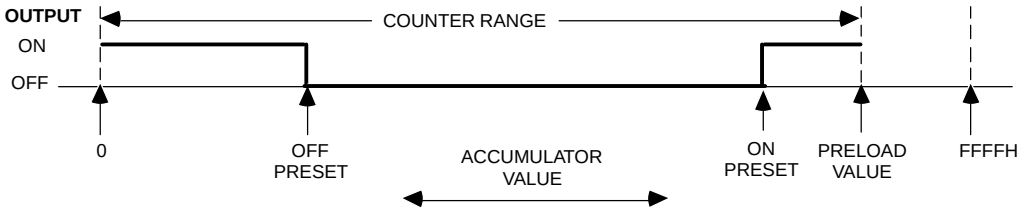
Standard Preset Output ON and OFF Positions

Each of the standard preset outputs has an ON and OFF preset value.



Location of Preset Points

Preset points may be located anywhere within the overall 0 to 65535 counting range. When the accumulator value is between the Preset points, the output ON / OFF state will always be that of the lowest Preset point. When the accumulator value is *not* between the Preset points, the output ON / OFF state will be that of the most positive preset. This is true regardless of the counter direction.



Interrupt on Preset ON and OFF Transitions

Each of the Preset Outputs has the capability to generate a ladder interrupt if this function is enabled in the configuration. For the Fast Preset Outputs interrupts may be enabled for the ON transition only. The Standard Preset Outputs interrupts can be enabled for either transition. Interrupts are disabled by default.

Count Mode

A counter can be configured to count continuously, automatically preloading when it reaches zero, or to count down to zero and stop.

Continuous counting

In continuous counting mode, the counter will automatically reload itself with the configured preload value when it reaches zero, and continue counting down.

Single-Shot counting

In Single-Shot mode, the counter will stop when it decrements to zero. Counting is enabled again when the counter is preloaded either by a %Q Preload Accumulator pulse or a pulse on the preload input.

Count Signal Mode

Each counter can be configured to interpret its Count inputs in one of two ways:

- Up / Down mode - rising edges on the A, or up, input increment the Accumulator while positive transitions on the B, or down, input decrement the Accumulator.
- A Quad B mode - if the A input leads the B input, the Accumulator is incremented and if the B input leads the A input the Accumulator is decremented.

Preload Value

For each counter, a starting, or Preload, value can be specified which will be used when the Preload input is activated. This Preload value is used for both hardware and software preloads. If the counter should be reset to 1000, use 1000 as the Preload value; this is the default value. The preload range is 1 to 65535.

Strobe Edge

Strobe inputs are edge sensitive. Each Strobe input on the module can be individually configured to have either the positive, negative, or both edges active. By default, they are positive edge sensitive.

Data Transfer Between High Speed Counter and CPU

The Series 90-70 High Speed Counter updates the %I and %AI data every 0.5 milliseconds. The Series 90-70 CPU reads this data immediately preceding each pass through the ladder logic, before triggering a ladder interrupt, and when a DOIO specifically requesting this data is performed in the ladder. To support the unique data coherency requirements of the High Speed Counter, the CPU reads both the %I and %AI data when performing a DOIO requesting only %I data.

The format of this input data depends on the counter configuration type. In return, during each I/O scan, the CPU sends 32 bits (%Q) of control data and 6 words (%AQ) of output data commands to the module. COMMREQ function blocks in the user program can be used to send additional data commands to the module.

See Appendix A for more information about COMMREQ and DOIO function blocks.

%I and %AI Data Sent by a Module Configured as Type E

The 32 status bits (%I) represent:

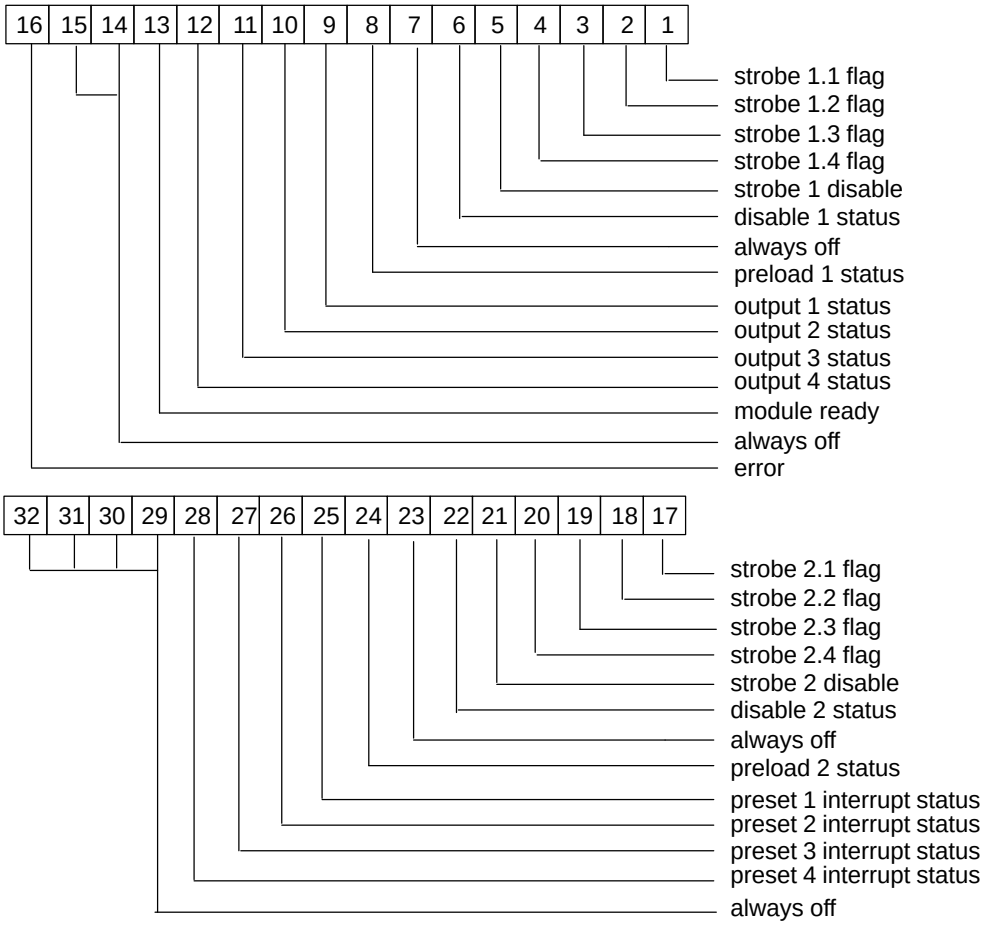
- Strobe status flags
- Strobe disable input status
- Count Disable input status
- Preload status
- Module ready status
- Error status
- Interrupt status

These status bits are sent to the CPU as inputs, and can influence outputs sent from the CPU to the module.

The 16 register data words (%AI) represent:

- Accumulators
- Strobes
- Module status code

Status Bits (%I) - Type E Counter



Strobe Status

Each bit indicates when a Strobe Pulse occurs on the counter. Each successive strobe causes the accumulator to be strobed into successive strobe registers, setting the corresponding strobe bit. If an application program uses these bits, it may clear them by setting the corresponding Reset Strobe %Q bit. The strobe status bits are reset automatically when the counter is preloaded by either a %Q or user input preload, or if the accumulator decrements to zero in continuous counting mode.

Strobe Disable Status

This bit indicates the level of the Strobe Disable input and whether strobing is disabled. When set, the Strobe Disable input is ON and strobe inputs are ignored.

Disable Status

This bit indicates the level of the Disable input and whether counting is disabled. When set, the Disable input is ON and count inputs are ignored.

Preload Status

This bit indicates that the counter has been preloaded by the terminal strip input, or that it has *rolled-under* in continuous mode. It is not set after a user has performed a %Q

preload. If an application program uses these bits, it may clear them by setting the corresponding Reset Preload %Q bit.

Output Status

These bits indicate the ON or OFF state of the four preset outputs.

Module Ready

This bit is set after the module completes its power-up tests.

Error Status

This bit is set when an error occurs. If it is set, a module status code has been returned in the first %AI location and the board OK LED flashes at 4 Hz. The Error Status bit is cleared by setting the Clear Error %Q bit.

Preset Interrupt Status

These bits are set by the HSC when the corresponding preset output has changed state, generating an interrupt. These flags may be used by an interrupt routine to indicate which counters have generated interrupts. The Output Status bits can be used in conjunction to determine which transition caused the interrupt. The Preset Interrupt Status bits should only be tested in a ladder interrupt handler.

%AI Data - Type E Counter

Word	Description
1	Module Status code
2	Accumulator for counter 1
3	Strobe 1 for counter 1
4	Strobe 2 for counter 1
5	Strobe 3 for counter 1
6	Strobe 4 for counter 1
7	Accumulator for counter 2
8	Strobe 1 for counter 2
9	Strobe 2 for counter 2
10	Strobe 3 for counter 2
11	Strobe 4 for counter 2
12 - 16	Unused

Module Status Codes

The Module Status Code in the %AI Input Data contains the error code returned to the PLC. The HSC sets this code to indicate a data command or configuration error. Once an error code has been returned, no more errors will be generated until the error is cleared. To clear a module status code, eliminate the condition that caused the error, and toggle the Clear Error %Q bit.

The Error code format and a list of error codes are given below.

High Byte		Low Byte
Error Source	Counter or Preset #	Error Code

Error Codes for Type E Counter

Error Code	Error Type	Definition
00	No error	No Error Present
11	Command Errors	Unknown Command
21		Invalid Counter or Preset
31		Invalid COMMREQ task ID
51		Outpulse ms out of range
98	Configuration Errors	Outpulse ms out of range
A8		Unsupported Feature Error
B8		Unknown Counter Type
C8		PLC Version Error
D8		Logicmaster 90 Version Error

Configuration Errors are not returned in %AI data since the module does not configure, but the error code is returned in the IO Fault data. The error data may be accessed by highlighting the fault in the I/O Fault Table and pressing the *Control* and *F* keys simultaneously.

Counter or Preset Number

For a valid command (recognized value in byte 0), the counter (1 or 2) or preset number, 1 to 4, which generated the error will be reported in this nibble. The Set Preset Accumulator command requires a valid preset and counter number or this value will be zero.

Error Source

Command errors return the source of the error.

Value	Error Source
1	%AQ Command 1 (%AQ Offset 0-2)
2	%AQ Command 2 (%AQ Offset 3-5)
4	COMMREQ Function

Example:

If the hexadecimal data 030A 0003 0000 was placed into the %AQ offsets 3 through 5 to try and set preset 3 to Counter 3, the error 2021h would be reported. The Module Status Code represents:

Value	Representation
2	Error in %AQ Command 2
0	Unknown Counter
21	Invalid Counter or Preset

%Q and %AQ Data Sent from CPU to HSC Configured as Type E

Once each I/O scan, the CPU sends eight words of data (32 bits of %Q and six words of %AQ) to the High Speed Counter Module. The application program can use these outputs to send commands to the module.

The 32 output bits (%Q) represent:

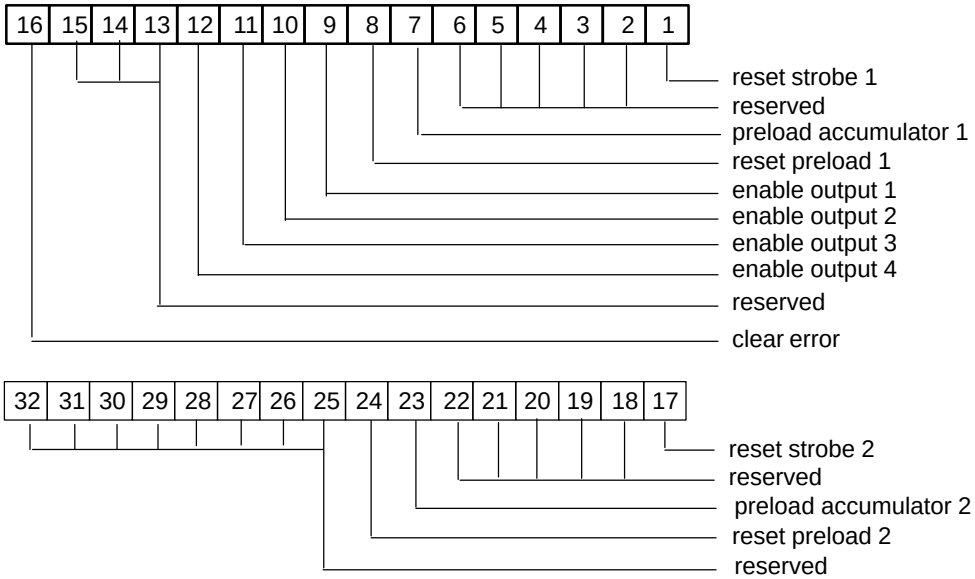
- Reset Strobes flag
- Accumulator Preload
- Reset Preload flag
- Output Enable
- Clear error

Six words (%AQ) of Command Data

The 6 words of command data, which can also be sent using a COMMREQ Function Block, can perform the following operations:

- Load Outpulse duration
- Set Preset Accumulators
- Load output preset on and off values
- Enable/Disable preset interrupts
- Load Preload values
- Load Oscillator divider

%Q Data - Type E Counter



Reset Strobe flag

This flag resets all the Strobe Status %I flags and allows up to four more strobes to be captured in the Strobe Stack. In the Type E, this bit is rising edge active, so new strobes can be captured while it is set.

Preload Accumulator

These bits tell the counter to perform a software preload and set the corresponding Accumulator to the Preload value. They do NOT, however, cause the corresponding Preload Status bit to be set.

Note

If a Strobe occurs between the time that a %Q Software Preload bit is set and when it is actually serviced by the counter, the Strobe value will be stored in the first available Strobe register, however the counter will reset the %I Strobe Status flags when it services the %Q Preload.

Reset Preload

This bit is used to clear the corresponding Preload Status %I bit. For example, if a Preload occurred, the Preload Status %I bit would be set. To clear this bit so future Preloads can be detected, the Reset Preload %Q bit must transition ON.

Clear Error

This bit should be set by the CPU to clear the Error Status %I bit after the error has been acknowledged. This bit is rising edge active, so new errors may appear while set.

Enable Output

These bits enable the corresponding preset output. If cleared, the output will always be OFF and not reflect the accumulator's value in relation to the Preset ON and OFF values.

Data Commands for Type E Counter

At the end of every CPU sweep, six words of %AQ data are automatically transferred from the CPU to the High Speed Counter. These six words are used to send data commands from the PLC to the HSC. The first three words, offsets 0 through 2, make up %AQ command 1, and the second three words, offsets 3 through 5, make up a completely separate %AQ command 2. Thus two commands can be sent to the HSC at the end of each sweep. Note that %AQ command 1 is executed first, so that if identical commands with different values are sent to the HSC simultaneously, %AQ command 2 data will overwrite %AQ command 1 data.

Even though the %AQ data is sent each sweep, commands are acted on ONLY if the command has changed since the last sweep. When any of the 6 bytes in a command changes, the HSC will accept the data as a new command and respond accordingly.

The DOIO function is supported, so that %AQ commands can be sent to the HSC mid-sweep. However, there must be 0.5 ms between a DOIO and the beginning or end of the sweep and between two DOIOs. This is to guarantee that the HSC has time to process each command before the data is overwritten by a subsequent command.

The COMMREQ function block can also be used to send data commands to the HSC mid-sweep. COMMREQs must be separated only from each other, and by at least 0.5 milliseconds. A description and example of the use of COMMREQs and DOIOs is given in Appendix A.

%Q data is processed by the HSC before the %AQ data. Therefore commands that can be affected by %Q bit operations should be sent at least one sweep before the %Q bit operation. For example, the Load Preload Value command should be sent one sweep before setting the Preload Accumulator %Q bit to preload that value.

In describing data commands, word offsets are shown in reverse order and in hexadecimal to simplify data entry. The following example sends Load Outpulse ms command with value 500 to counter 2 using offsets 0 through 2.

The first word, or command word, which goes into word offset 0 would be 0209h. The value 09 in byte 0 represents the command Load Outpulse ms command. The value 02 in byte 1 is the counter number, in this case counter 2. For the Load Outpulse ms command, word 1 is the value to be configured and word 2 is ignored. In this example, word 1 would have the value 500 (1F4h) because that is the value to be configured. Word 2 will be ignored but should be set to 0. If word offset 0 corresponded to %AQ1, the complete command to load the counter 2 accumulator with value 0001 would be:

%AQ3 (word 2)	%AQ2 (word 1)	%AQ1 (word 0)
0000	01F4	0209

The following table is a list of data commands for counter Type E. Byte 0 data is in hexadecimal format.

Command Definition	Data				Command Word	
	Word 2		Word 1		Word 0	
	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
Null	xx	xx	xx	xx	xx	00h
Load Outpulse ms	xx	xx	data (16)		n	09h
Set Preset Accumulator	xx	xx	xx	data (8)	k	0Ah
Load Preset ON Value	xx	xx	data (16)		k	0Bh
Enable/Disable Preset ON Interrupt	xx	xx	xx	data (8)	m	0Fh
Load Preset OFF Value	xx	xx	data (16)		k	15h
Enable/Disable Preset OFF Interrupt	xx	xx	xx	data (8)	k	19h
Load Preload Value	xx	xx	data (16)		n	1Fh
Load Oscillator Divider	xx	xx	data (16)		0	32h

k = Preset Number (3, 4); m = Preset Number (1 to 4); n = Counter Number (1, 2);
xx = Do not care (ignored); data (8, 16, 24) = 8, 16, or 24 bit data

Descriptions of each command are given below. The valid range of values is given in parenthesis.

Null

This is the default %AQ data command. Since the %AQ data is transferred each PLC sweep, it is a good idea to have the Null command present when not executing a specific data command to avoid inadvertent execution. All data is ignored with a Null command.

Load Outpulse ms (1 to 1000)

This command sets the fast preset output pulse duration when configured for pulse mode operation. The value must be in the range of 1 to 1000, or an error will be returned and the command ignored.

Note

When configured for continuous counting with pulsed outputs, the configured pulse duration must be at least .75 milliseconds less than the time required to count from the preload down to zero. This is to ensure that the output has had time to turn off before being set again.

Preset Accumulator (0, 1 or 2, presets 3 and 4 only)

This command sets the accumulator referenced by the standard preset outputs. A data value of 0 disables the corresponding output.

Load ON and OFF Preset Value (0 to 65535, presets 3 and 4 only)

This command sets the preset output turn on and turn off points. Preset values can be any value in the range of 0 to 65535.

Enable/Disable Preset ON and OFF Interrupts. (0=Disable, 1=Enable)

This command enables or disables interrupts resulting from Preset output transitions. For example, if Preset ON interrupts are enabled, then a low to high transition of the Preset ON output will generate an interrupt to the CPU. This command allows the interrupts to be enabled or disabled within a ladder. The OFF interrupt is only supported by the standard preset outputs (3 and 4).

Load Preload Value (1 to 65535)

The Load Preload command sets the value to which the Accumulator will be set when a positive edge occurs on the Preload input, the %Q Preload bit is set, or the counter *rolls-under* in continuous mode.

Load Oscillator Divider (1 to 65535)

This command changes the frequency of the square wave oscillator signal. The frequency generated is 1 megahertz (1 MHz) divided by the oscillator divider. Thus to get 50 Hz, the oscillator divider should be 20000.

Appendix A Using Special CPU Communications Functions

The Series 90-70 High Speed Counter has some operational requirements that are unique among the Series 90-70 I/O products. To better support these requirements, the Series 90-70 COMMREQ and DOIO Function blocks have some special characteristics which are described here.

Sending Data Commands Using the COMMREQ Function

Data commands sent using %AQ data are not processed by the HSC until the %AQ data is transmitted, either at the end of the ladder sweep or when a DO I/O command forces a mid-sweep update of the %AQ HSC data. For large ladders, the COMMREQ function provides a mechanism for sending Data Commands mid-sweep which will be processed immediately by the HSC.

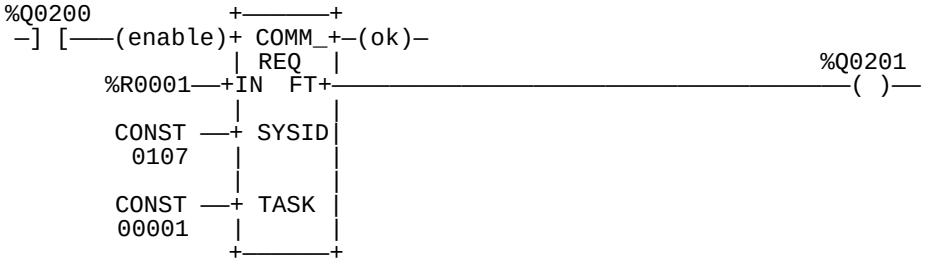
The PLC ladder program sends a Data Command using the COMMREQ (Communications Request) function. The COMMREQ requires that all its command data be placed in the correct order in the CPU memory before it is executed. It should then be executed by a one-shot to prevent sending the data to the High Speed Counter multiple times. Successive COMMREQs must be separated by at least 0.5 milliseconds to guarantee correct processing by the HSC. A description of the COMMREQ function and its command block data follows along with a ladder example which uses registers %R0001 to %R0009 for the COMMREQ command block. Refer to GFK-0265, the *Series 90-70 Programmable Controller Reference Manual*, for additional specific information on COMMREQs.

COMMREQ Function Block Description

The Communications Request (COMMREQ) function is a conditionally executed function that communicates a particular request, through the ladder logic program, to the High Speed Counter.

Communications Request Function Block Format

The ladder logic representation of the COMMREQ is as follows:



The Communications Request function block has four inputs and two outputs. The first input is an enable input. Generally a one-shot coil is used to enable the COMMREQ function. This prevents multiple messages from being sent. The second input (IN) is the starting location of the COMMREQ command block. The SYSID input is used to indicate which rack and slot to send the message to (physical location of High Speed Counter module). In the above example, the SYSID 0107 (in Hexadecimal) points to rack 1, slot 7 and the COMMREQ command block starts at Register 0001. The last input (TASK) must be set to a 1.

Power is always passed to the ok output. The fault output (FT) is enabled if the COMMREQ fails.

Command Block

The command block for data Commands is composed of 9 words of information arranged in the following fashion: (all values in hexadecimal unless otherwise indicated). Use the block move command to move these values to the Register tables (refer to the *Series 90-70 Programmable Controllers Reference Manual*, GFK-0265, for information on using the block move function).

Location	Data	Description
%R0001	0003	Length of data is three words
%R0002	0000	Not used (Always zero)
%R0003	0000	Not used
%R0004	0000	Not used
%R0005	0000	Not used
%R0006	0000	Not used
%R0007	nnnn	Data Command - Command Word - Word 0
%R0008	nnnn	Data Command - Command Word - Word 1
%R0009	nnnn	Data Command - Command Word - Word 2

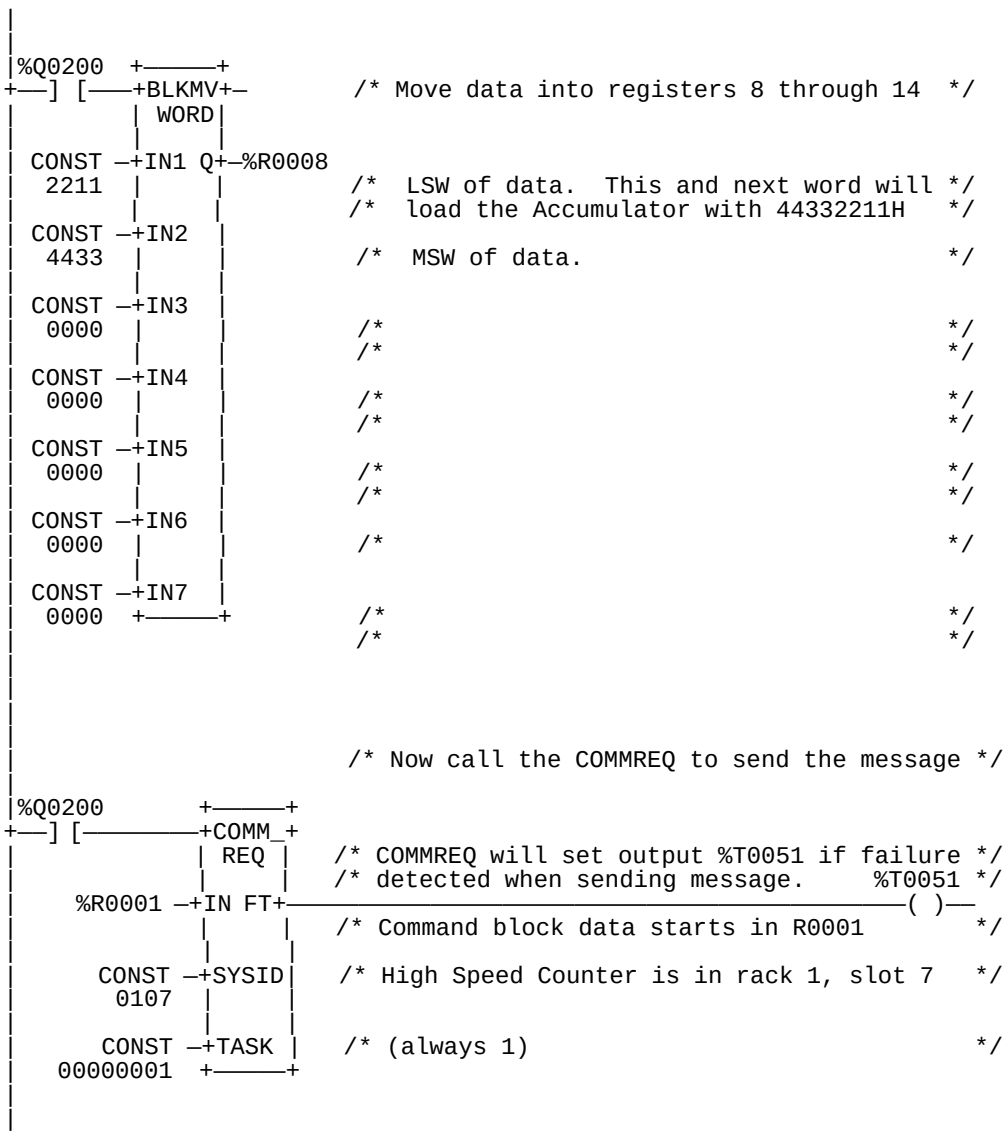
Example - Sending Data Commands

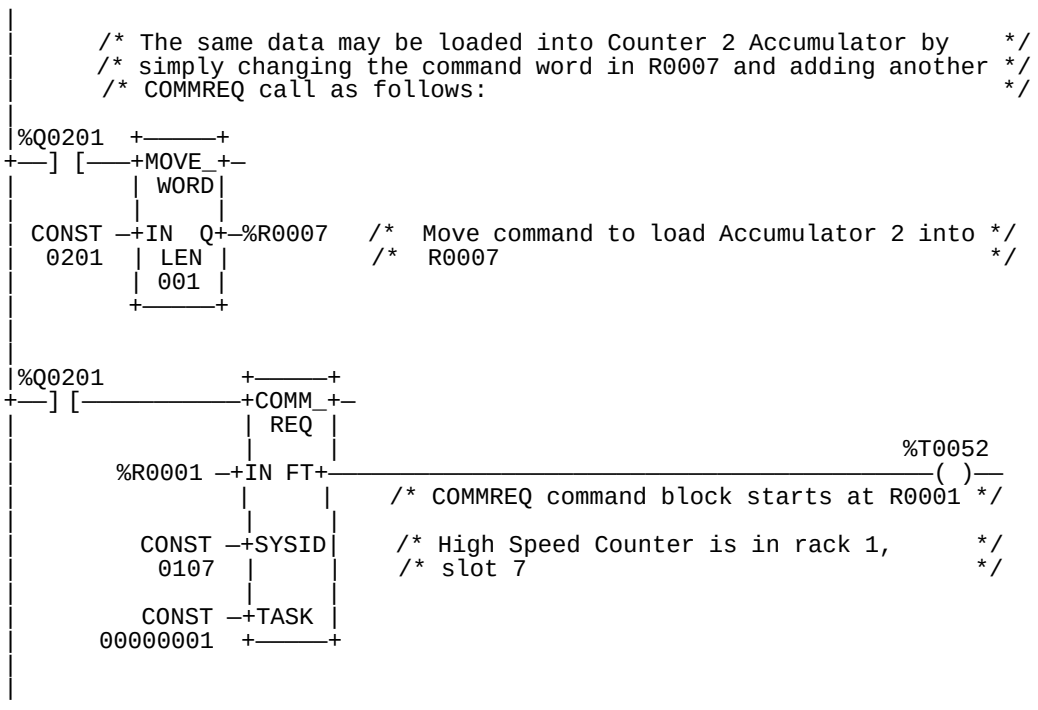
An example of ladder logic for sending a data command to a Type B High Speed Counter using COMMREQ function blocks is shown below. In this example, the COMMREQ command block is located in registers %R0001 through %R0009. The command to send the data is initiated by the conditional input %I0289 which sets output %Q0200 for one sweep. The High Speed Counter is located in Rack 1, slot 7 (first expansion rack). This command will load Accumulator 1 with the value 44332211h.

If the COMMREQ command data is formatted incorrectly, or has an invalid command, the HSC will set the Error Status %I bit, and return an error code in Module Status Code %AI word.

Note that the comments within / . . . . */ have been included for information purposes only. They are not generated by the Logicmaster 90 software.*

```
|
|%I0289                                                          %Q0200
+--][-------------------------------------------------------------(P)--
|
|%I0290                                                          %Q0201
+--][-------------------------------------------------------------(P)--
|
|%Q0200  +------+
+--] [---+BLKMV+-       /* Move Command block into Registers 1-7  */
|        | WORD|
|        |     |
| CONST -+IN1 Q+-%R0001  /* Command block data starts at %R0001    */
|  0003  |     |         /* Command data is 3 words                */
|        |     |         /*
| CONST -+IN2  |
|  0000  |     |         /* Not used (always 0000)                */
|        |     |
| CONST -+IN3  |
|  0000  |     |         /* Not used (always 0000)                */
|        |     |
| CONST -+IN4  |
|  0000  |     |         /* Not used (always 0000)                */
|        |     |
| CONST -+IN5  |
|  0000  |     |         /* Not used (always 0000)                */
|        |     |
| CONST -+IN6  |
|  0000  |     |         /* Not used (always 0000)                */
|        |     |
| CONST -+IN7  |
|  0101  +------+         /* First word (Command Word)            */
|                        /* In this case, load Accumulator 1      */
|
```


%Q0200
BLKMV
WORD
CONST 2211
IN1
%R0008
CONST 4433
IN2
CONST 0000
IN3
CONST 0000
IN4
CONST 0000
IN5
CONST 0000
IN6
CONST 0000
IN7
/* Move data into registers 8 through 14 */
/* LSW of data. This and next word will */
/* load the Accumulator with 44332211H */
/* MSW of data. */
/* Now call the COMMREQ to send the message */
%Q0200
COMM_
REQ
%R0001
IN
FT
%T0051
/* COMMREQ will set output %T0051 if failure */
/* detected when sending message. %T0051 */
/* Command block data starts in R0001 */
CONST 0107
SYSID
/* High Speed Counter is in rack 1, slot 7 */
CONST 00000001
TASK
/* (always 1) */


/* The same data may be loaded into Counter 2 Accumulator by */
/* simply changing the command word in R0007 and adding another */
/* COMMREQ call as follows: */
%Q0201
MOVE
WORD
CONST
0201
IN
Q
LEN
001
%R0007
/* Move command to load Accumulator 2 into */
/* R0007 */
%Q0201
COMM
REQ
%R0001
IN
FT
%T0052
/* COMMREQ command block starts at R0001 */
CONST
0107
SYSID
/* High Speed Counter is in rack 1, */
/* slot 7 */
CONST
00000001
TASK

Updating I/O Data using the DOIO Function

The DO I/O function is used to update selected inputs or outputs for one scan, in addition to the normal I/O scan, while the program is running.

In the High Speed Counter there is a close relationship between the Status (%I) data and the Counter (%AI) data. Status bits reflect events that change the Counter Data, such as Preloads, Strobes, and Disables. In addition, changes in the Counter Data can cause Status Data to change, such as when an Accumulator reaches a Preset position. To support this close correlation between the Status and Counter data, the DOIO function provides a means for updating both Discrete and Analog tables coherently, using a single DOIO function block.

DOIO Function Block Format

The ladder logic representation of the DOIO is as follows:

The DOIO function has four input parameters and one output parameter. When the function receives power flow and input references are specified, the input points starting at the reference ST and ending at END are scanned. If a discrete (%I) reference is specified, with no alternate destination, both the Status (%I) and Counter (%AI) data for the referenced counter(s) are updated. Because this operation involves the transfer of two tables, it is only supported when no alternate location is specified. If a reference is specified for ALT, a copy of the new input values is placed in memory beginning at the alternate reference, and the real input points are not updated; however only the specified table is copied. The DOIO function block represented in the figure above will update both the %I and %AI data for a HSC with a %I starting reference of %I00001.

When the DOIO function receives power flow and output references are specified, the output points starting at the reference ST and ending at END are written to the referenced counter module(s). If outputs should be written to the output modules from internal memory other than %Q or %AQ, the beginning reference can be specified using the ALT input. If a discrete (%Q) reference is specified with no alternate source both the Control (%Q) and Command (%AQ) data are updated using the referenced High Speed Counter's %Q and %AQ data. Thus the DOIO function block represented in the figure above will transfer 32 bits of discrete data from the alternate source location starting at %T1 to the HSC configured with %Q starting reference of %Q00001.

Refer to GFK-0265, *the Series 90-70 Programmable Controller Reference Manual*, for additional specific information on the DOIO Function Block.

Appendix B Using Interrupts with the HSC

This appendix provides a description of how to use interrupts with the High Speed Counter.

Caution

An I/O interrupt can interrupt the execution of a function block in any program block, including the _MAIN block. Therefore, unexpected results may occur if the interrupt block and a program block access the same data. When it is necessary for an interrupt block and a program block to access the same data, a SVCREQ #17 or SVCREQ #32 can be used to temporarily block the interrupt from executing when the shared data is being accessed.

High Speed Counter Interrupt Capability

The High Speed Counter can be configured to generate a ladder interrupt to the Series 90-70 CPU when any of the Preset Outputs change state. This capability provides a means to minimize the latency for any special service to be performed when an Output transitions. Correct use of the interrupt capability requires care, and a good understanding of the HSC and CPU operation and interaction.

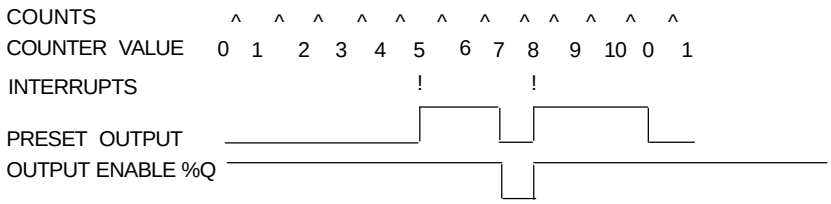
The High Speed Counter has four Preset Outputs, each tied to a hardware output with an LED indicator. When configured for Type A, B, C, or D operation interrupts can be enabled or disabled for either or both edges of each of the Preset Outputs. When configured for Type E operation the High Speed Counter has two High Speed Outputs and two Standard Preset Outputs. Interrupts can be enabled for the off-to-on transition of the High Speed Outputs. Interrupts for the Standard Outputs are identical to the other counter types.

Interrupt Operation

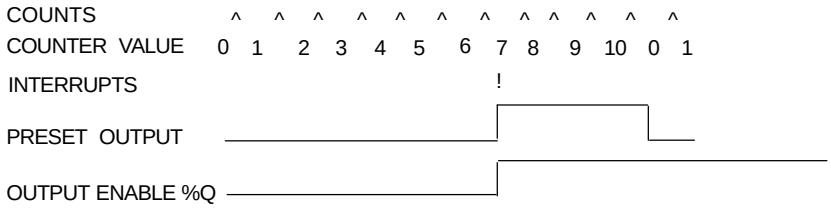
When a Preset Output changes state, and the corresponding interrupt is enabled, the High Speed Counter will transmit the current %I and %AI data to the CPU. Upon receipt of the data, the CPU will suspend its current activity, update the %I and %AI data for the HSC, and then execute the interrupt logic. The execution of a block triggered from an interrupt supersedes the execution of the main program sequence. Execution of the main sequence is resumed after the interrupt block completes.

Any transition of an output for which the interrupt is configured as enabled will cause an interrupt to be generated. For example, if an output has its On Preset set to 5, Off Preset set to 10, the On Interrupt enabled, and the associated Output Enable %Q bit is on, the counter will generate an interrupt when the accumulator increments to 5. If the output is then pulsed off and back on by toggling the Output Enable %Q bit, the on transition of the output will generate an interrupt.

Count Limits:	*0 - 10*	*Preset On Interrupt:*	*Enabled*
On Preset:	*5*	*Preset Off Interrupt:*	*Disable*
Off Preset:	*10*		



Likewise, if the Output Enable %Q bit is off, and the counter is incremented into the preset on range, the output will not turn on and no interrupt will be generated until the Output Enable %Q bit is set. For example, if the counter is configured as in the example above, except the %Q Output Enable bit is not set until the counter reaches 7. In this case, the output won't turn on, and no interrupt will be generated until the %Q bit has turned on.



CPU Interrupt Routine

If a High Speed Counter has interrupts enabled for any output, a Ladder interrupt logic block must be defined for that module. If an interrupt logic block is not defined, the Series 90-70 CPU will report a fault. The CPU supports one interrupt logic block for each HSC module. When defining the interrupt logic block, the first %I reference of the HSC must be specified as the trigger reference. Four %I bits (%I25 - %I28) contain the HSC interrupt status. Each bit corresponds to one of the Preset Outputs and is set when the corresponding Output generated the interrupt.

The Preset Output status bits (%I9 - %I12) indicate the current Preset Output state so the interrupt logic can determine which edge(s) occurred. If multiple outputs transition within a single .5 mS counter service cycle, all the corresponding interrupt status bits will be set and only one interrupt will be generated. The interrupt status bits are only set when an HSC interrupt is generated, and should not be tested outside the counter interrupt logic block.

Controlling Interrupts

Interrupts can occur at any time with respect to the CPU sweep. Because of this asynchronous nature and the automatic update of %I and %AI data, it is necessary to temporarily suspend or disable the interrupts surrounding function blocks that operate on the %I or %AI data. An example is a _MAIN ladder block performing comparisons against %AI data from a counter which is generating interrupts. If an interrupt occurs while the Compare function block is executing, the data can be changed in the midst of the compare rendering the results invalid. To prevent this, interrupts need to be disabled or suspended surrounding the compare function. The Series 90-70 CPU provides two mechanisms for controlling interrupts.

Masking Interrupts

In PLC ladder, a Service Request #17 function block may be used to mask and unmask interrupts from the High Speed Counter. When this service request is active the CPU will ignore any interrupts from the specified counter and I/O will update normally, as if no interrupts had been configured for the module. **The Service Request #17 status is maintained in the retentive CPU memory, and will remain active even if the CPU is power-cycled.** Service Request #17 has a three word parameter block that specifies whether interrupts are to be enabled or disabled, and identifies the device for which interrupts are to be disabled.

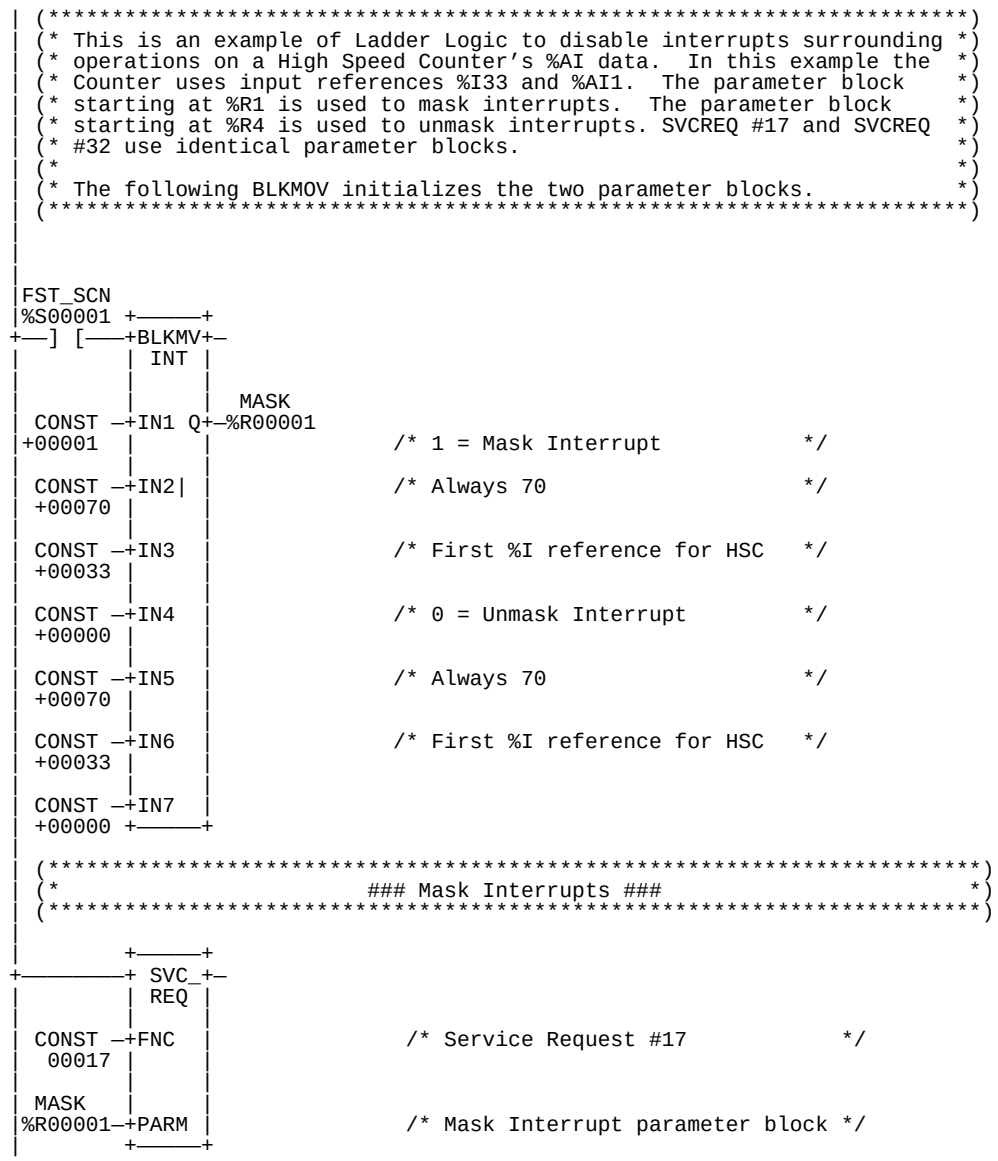
Table B-1. Service Request #17 Parameter Block

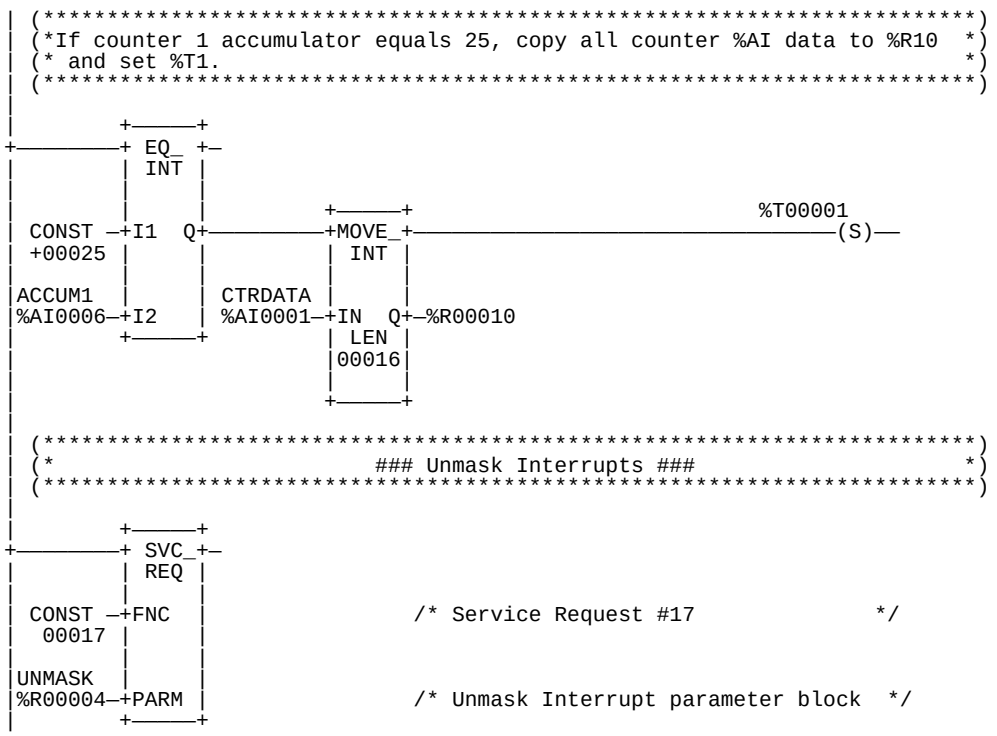
Offset	Description
Address	0 = Interrupts Unmasked 1 = Interrupts Masked
Address + 1	70
Address + 2	First %I reference of selected HSC

Example of Ladder Logic

The following pages contain an example of Ladder logic that initializes two parameter blocks, and masks interrupts for a High Speed Counter whose %I data starts at %I33. Interrupts are then unmasked after the compare and move function.

Note that the comments within / . . . . */ have been included for information purposes only. They are not generated by the Logicmaster 90 software.*


(***)
(* This is an example of Ladder Logic to disable interrupts surrounding *)
(* operations on a High Speed Counter's %AI data. In this example the *)
(* Counter uses input references %I33 and %AI1. The parameter block *)
(* starting at %R1 is used to mask interrupts. The parameter block *)
(* starting at %R4 is used to unmask interrupts. SVCREQ #17 and SVCREQ *)
(* #32 use identical parameter blocks. *)
(* *)
(* The following BLKMOV initializes the two parameter blocks. *)
(***)
FST_SCN
%S00001
BLKMV
INT
MASK
CONST
+00001
IN1
Q
%R00001
/* 1 = Mask Interrupt */
CONST
+00070
IN2
/* Always 70 */
CONST
+00033
IN3
/* First %I reference for HSC */
CONST
+00000
IN4
/* 0 = Unmask Interrupt */
CONST
+00070
IN5
/* Always 70 */
CONST
+00033
IN6
/* First %I reference for HSC */
CONST
+00000
IN7
(***)
(* ### Mask Interrupts ### *)
(***)
SVC_REQ
CONST
00017
FNC
/* Service Request #17 */
MASK
%R00001
PARM
/* Mask Interrupt parameter block */



Suspending Interrupts

The Service Request #32 function block may be used to temporarily suspend interrupts from the High Speed Counter. It differs from Service Request #17 in that interrupts occurring while a Suspend is active will be stored, and transmitted to the CPU as soon as the Suspend is disabled. A maximum of 15 interrupts are stored by the HSC in a circular queue. If more than one interrupt occurs during a Suspend, each interrupt is queued by the HSC. When the Suspend is deactivated, each queued interrupt is sent to the CPU one at a time, in the order of occurrence, as fast as the CPU can service them. If more than 15 interrupts occur during suspension, the oldest interrupts are removed from the head of the queue, and new interrupts are added to the tail. Thus, only the 15 newest interrupts are reported to the CPU when the suspend is disabled.

The Suspend / Unsuspend Interrupts service requests are designed to be placed around locations in the ladder logic which reference HSC %I and %AI data. If interrupts are suspended before operations using the HSC data begins, the HSC data will not be changed during the operations. If the interrupts are not suspended, comparisons and calculations can start using one set of data, an interrupt could occur which updates and changes the data, and the calculations would use altered data when the interrupt routine completed.

Interrupts should NEVER be suspended from the end of a ladder sweep to the beginning of the next sweep. %I and %AI data updates are disabled when interrupts are suspended to ensure that all data is reported to the CPU in the same sequence it occurred at the HSC.

Note

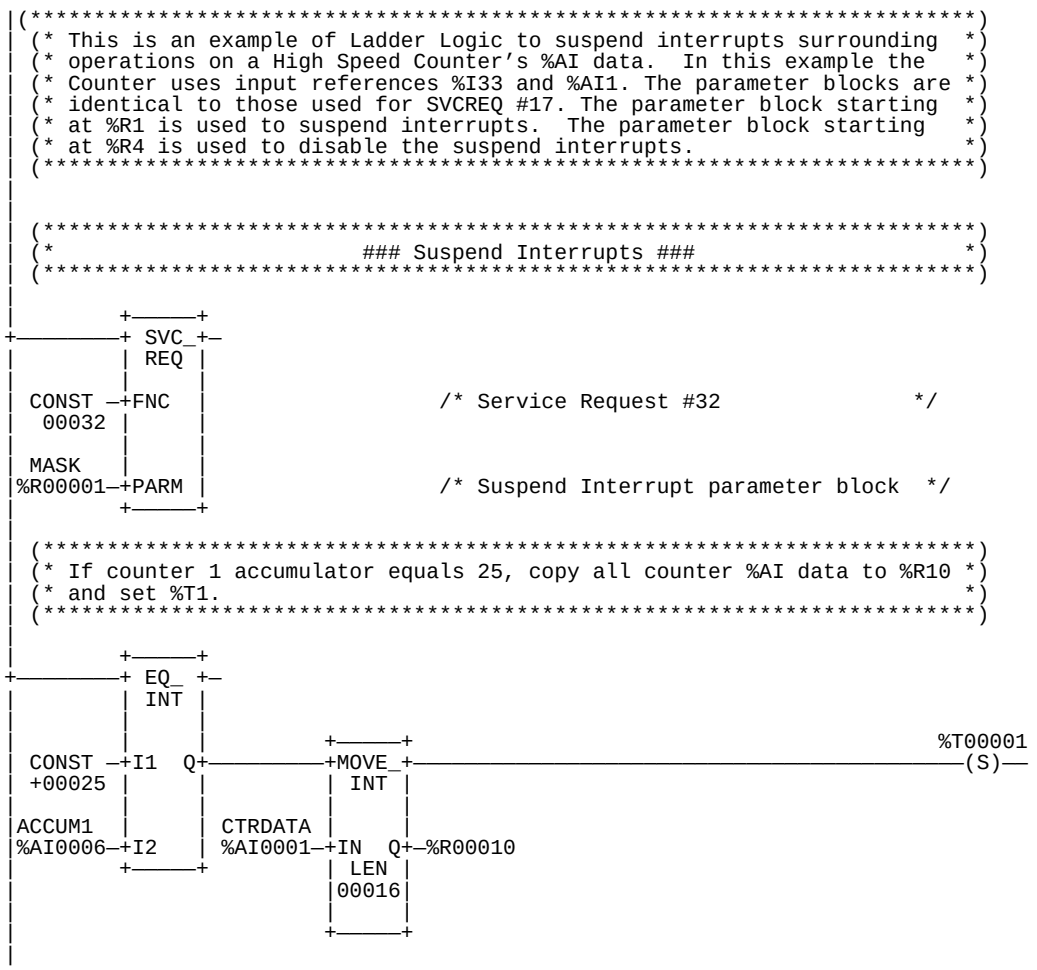
Service Request #32 status is not retained through a power-cycle. If the rack containing the CPU or the HSC are power-cycled, the SVCREQ #32 is deactivated, and interrupts will be generated normally.

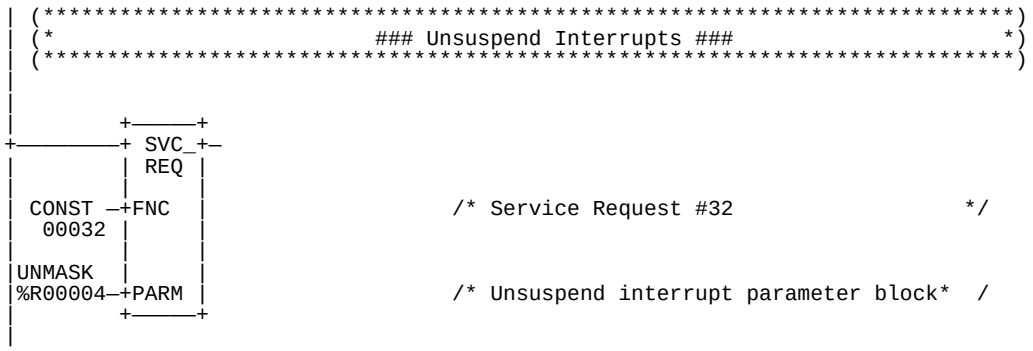
Example of Ladder Logic

Following is an example of Ladder logic that suspends interrupts for a High Speed Counter whose %I data starts at %I33. The Interrupts suspend is disabled after the compare and move functions. The parameter blocks for SVCREQ #32 are identical to those used for SVCREQ #17.

For this example, assume that the parameter blocks have been uninitialized as in the previous example.

Note that the comments within / . . . . */ have been included for information purposes only. They are not generated by the Logicmaster 90 software.*





Suggestions for Using Interrupts

The following is a list of suggestions for using the Series 90-70 High Speed Counter interrupt capability.

- Place Suspend / Unsuspend Interrupt service requests before and after any rungs which access the HSC %I and %AI locations.
- Minimize the time during which interrupts are masked or suspended. If interrupts are almost always suspended or masked, they serve no purpose.
- If there are numerous or lengthy ladder operations using the %I or %AI data, suspend interrupts around a rung which copies the %I and %AI data to alternate locations. The ladder then can use the alternate locations without data coherency problems and the interrupt routine can use the real %I and %AI locations. This procedure can be repeated as necessary throughout the ladder.
- Always disable an interrupt suspend (#SVCREQ 32) before the end of the ladder sweep.

Appendix C

High Speed Counter Summary

This appendix provides a summary of the Series 90-70 High Speed Counter. Applicable data is listed for each counter type.

High Speed Counter %I Return Data

Bit	Counter Type A	Counter Type B	Counter Type C	Counter Type D	Counter Type E
1	Strobe 1 Flag	Strobe 1.1 Flag	Strobe 1 Flag	Home 1 Found	Strobe 1.1 Flag
2	Strobe 2 Flag	Strobe 1.2 Flag	Strobe 2 Flag	Home 2 Found	Strobe 1.2 Flag
3	Strobe 3 Flag	Strobe 2.1 Flag	Strobe 3 Flag	Home 3 Found	Strobe 1.3 Flag
4	Strobe 4 Flag	Strobe 2.2 Flag	Home Found	Home 4 Found	Strobe 1.4 Flag
5	Preload 1 Flag	Preload 1 Flag	Preload 1 Flag	Alwaysoff	Strobe 1 Disable
6	Preload 2 Flag	Preload 2 Flag	Preload 2 Flag	Alwaysoff	Disable 1 Status
7	Preload 3 Flag	Disable 1 Status	Disable Status	Alwaysoff	Alwaysoff
8	Preload 4 Flag	Disable 2 Status	Home Status	Alwaysoff	Preload 1 Status
9 - 12	Output 1 - 4 Status				
13	Module Ready				
14 - 15	Alwaysoff				
16	Error Flag				
17	Alwaysoff				Strobe 2.1 Flag
18	Alwaysoff				Strobe 2.2 Flag
19	Alwaysoff				Strobe 2.3 Flag
20	Alwaysoff				Strobe 2.4 Flag
21	Alwaysoff				Strobe 2 Disable
22	Alwaysoff				Disable 2 Status
23	Alwaysoff				
24	Alwaysoff				Preload 2 Status
25 - 28	Preset 1 - 4 Interrupt Status				
29 - 32	Alwaysoff				

High Speed Counter %AI Return Data

Word	Counter Type A	Counter Type B	Counter Type C	Counter Type D	Counter Type E
1	Module Status Code				
2	Cts / Tmebase 1	Cts / Tmebase 1	Cts / Tmebase 1	Cts / Tmebase 1	Accumulator1
3	Cts / Tmebase 2	Cts / Tmebase 2	Always0000	Cts / Tmebase 2	Strobe 1.1
4	Cts / Tmebase 3	Accumulator1	Accumulator	Cts / Tmebase 3	Strobe 1.2
5	Cts / Tmebase 4			Cts / Tmebase 4	Strobe 1.3
6	Accumulator1	Strobe Reg 11	Strobe Reg 1	Accumulator1	Strobe 1.4
7	Strobe Reg 1				Accumulator2
8	Accumulator2	Strobe Reg 12	Strobe Reg 2	Accumulator2	Strobe 2.1
9	Strobe Reg 2				Strobe 2.2
10	Accumulator3	Accumulator2	Strobe Reg 3	Accumulator3	Strobe 2.3
11	Strobe Reg 3				Strobe 2.4
12	Accumulator4	Strobe Reg 21	Always0000	Accumulator4	Always0000
13	Strobe Reg 4		Always0000		Always0000
14	Always0000	Strobe Reg 22	Always0000	Always0000	Always0000
15	Always0000		Always0000	Always0000	Always0000
16	Always0000				

High Speed Counter %Q Control Data

Bit	Counter Type A	Counter Type B	Counter Type C	Counter Type D	Counter Type E
1	Reset Strobe 1	Reset Strobe 1.1	Reset Strobe 1	Home Command 1	Reset Strobes (1)
2	Reset Strobe 2	Reset Strobe 1.2	Reset Strobe 2	Home Command 2	Reserved
3	Reset Strobe 3	Reset Strobe 2.1	Reset Strobe 3	Home Command 3	Reserved
4	Reset Strobe 4	Reset Strobe 2.2	Reserved	Home Command 4	Reserved
5	Reset Preload 1	Reset Preload 1	Reset Preload 1	Reserved	Reserved
6	Reset Preload 2	Reset Preload 2	Reset Preload 2	Reserved	Reserved
7	Reset Preload 3	Reserved	Reserved	Reserved	Preload Acc 1
8	Reset Preload 4	Reserved	Reserved	Reserved	Reset Preload 1
9	Enable Output Preset 1				
10	Enable Output Preset 2				
11	Enable Output Preset 3				
12	Enable Output Preset 4				
13	Reserved				
14	Reserved	Reserved	Home Command	Reserved	Reserved
15	Reserved				
16	Clear Error				
17	Preload Acc 1	Preload Acc 1	Acc Preload 1	Preload Acc 1	Reset Strobes (2)
18	Preload Acc 2	Preload Acc 2	Acc Preload 2	Preload Acc 2	Reserved
19	Preload Acc 3	Reserved	Reserved	Preload Acc 3	Reserved
20	Preload Acc 4	Reserved	Reserved	Preload Acc 4	Reserved
21 - 22	Reserved				
23	Reserved	Reserved	Reserved	Reserved	Preload Acc 2
24	Reserved	Reserved	Reserved	Reserved	Reset Preload 2
25 - 32	Reserved				

High Speed Counter Data Commands

Command Definition	Command Data				Command Word		Applicable Counters
	Word 2		Word 1		Word 0		
	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0	
Null	xx	xx	xx	xx	xx	00h	A - E
Load Accumulator Value	data (16 or 32)				n	01h	A - D
Load High Limit	data (16 or 32)				n	02h	A - D
Load Low Limit	data (16 or 32)				n	03h	A - D
Load Accumulator Increment	xx	xx	xx	data (8)	n	04h	A - D
Load Counter Direction	xx	xx	xx	data (8)	n	05h	A
Load Timebase	xx	xx	data (16)		n	06h	A - D
Load Velocity Increment	xx	data (24)			n	07h	A - D
Load Home Value	data (32)				n	08h	C, D
Load Outpulse ms	xx	xx	data (16)		n	09h	E
Set Preset Accumulator	xx	xx	xx	data (8)	k	0Ah	E
Load Preset ON Value	data (16 or 32)				m	0Bh	All
Enable / Disable Preset ON Interrupt	xx	xx	xx	data (8)	m	0Fh	All
Load Preset OFF Value	data (16 or 32)				m	15h	All
Enable / Disable Preset OFF Interrupt	xx	xx	xx	data (8)	m	19h	All
Load Preload Value	data (16 or 32)				n	1Fh	All
Load Preload 2 Value	data (32)				n	20h	C
Load Oscillator Divider	xx	xx	data (16)		0	32h	All

k = Preset Number (3 to 4); m = Preset Number (1 to 4); n = Counter Number (1, 2);
xx = Do not care (ignored); data (8, 16, 24) = 8, 16, or 24 bit data

High Speed Counter Module Status Codes (%AI Word 1)

Nibble 3	Nibble 2	Nibble 1	Nibble 0
Error Source	*Counter/Preset #*	*Error Descriptor*	*Main Error Code*
0	0	0	0 = No Error
1 = %AQ1 - 3 2 = %AQ4 - 6 4 = COMMREQ 8 = Configuration	0	1 = Unknown Command	1 = Command Error
		2 = Invalid Counter / Preset	
		3 = Invalid COMMREQ Task ID	
	1 = Counter 1 2 = Counter 2 3 = Counter 3 4 = Counter 4	4 = Velocity Increment Out of Range	
		5 = Outpulse ms Out of Range	
		8 = Accumulator Out of Range	
		9 = Preload Value Out of Range	
		A = Preload 2 Value Out of Range	
		B = Home Value Out of Range	
	Preset Number	C = Preset ON Out of Range	
		D = Preset Off Out of Range	
	1 = Counter 1 2 = Counter 2 3 = Counter 3 4 = Counter 4	1 = High Limit < Low Limit	2 = Command Limit Error
		2 = Range Excludes Preload	
		3 = Range Excludes Preload 2	
		4 = Range Excludes Home	
		5 = Range Excludes Preset ON	
		6 = Range Excludes Preset OFF	
0	1 = Counter 1 2 = Counter 2 4 = Counter 3 8 = Counter 4	0	4 = Home Error
			5 = Quadrature Error
0	0 = Non Counter Specific 1 = Counter 1 2 = Counter 2 3 = Counter 3 4 = Counter 4	1 = High Limit < Low Limit	8 = Configuration Error
		2 = Range Excludes Preload	
		3 = Range Excludes Preload 2	
		4 = Range Excludes Home	
		5 = Range Excludes Preset ON	
		6 = Range Excludes Preset OFF	
		9 = Outpulse ms Out of Range	
		A = Unsupported Feature Error	
		B = Unknown Counter Type Error	
		C = PLC Version Error	
		D = Logicmaster 90 Version Error	

High Speed Counter User I/O Terminal Pin Assignments

The following table defines which terminals to use for the type of counter selected during module configuration.

Connector Pin Number	Signal Name	Use in Counter Type				
		Type A	Type B	Type C	Type D	Type E
1	IN1P	CH1P	CH1AP	CH1AP	CH1AP	CH1AP
2	IN2P	CH2P	CH1BP	CH1BP	CH1BP	CH1BP
3	IN1M	CH1M	CH1AM	CH1AM	CH1AM	CH1AM
4	IN2M	CH2M	CH1BM	CH1BM	CH1BM	CH1BM
5	IN3P	CH3P	CH2AP	CH2AP	CH2AP	CH2AP
6	IN4P	CH4P	CH2BP	CH2BP	CH2BP	CH2BP
7	IN3M	CH3M	CH2AM	CH2AM	CH2AM	CH2AM
8	IN4M	CH4M	CH2BM	CH2BM	CH2BM	CH2BM
11	IN5P	PRLD1P	PRLD1P	PRLD1P	CH3AP	PRLD1P
12	IN6P	PRLD2P	DISABLE1P	DISABLE1P	CH3BP	DISABLE1P
13	IN5M	PRLD1M	PRLD1M	PRLD1M	CH3AM	PRLD1M
14	IN6M	PRLD2M	DISABLE1M	DISABLE1M	CH3BM	DISABLE1M
15	IN7P	PRLD3P	PRLD2P	PRLD2P	CH4AP	PRLD2P
16	IN8P	PRLD4P	DISABLE2P	HOMEP	CH4BP	DISABLE2P
17	IN7M	PRLD3M	PRLD2M	PRLD2M	CH4AM	PRLD2M
18	IN8M	PRLD4M	DISABLE2M	HOMEM	CH4BM	DISABLE2M
21	IN9P	STRB1P	STRB11P	STRB11P	MRKR1P	STRB1P
22	IN10P	STRB2P	STRB12P	STRB12P	MRKR2P	STRBDIS1P
23	IN9M	STRB1M	STRB11M	STRB11M	MRKR1M	STRB1M
24	IN10M	STRB2M	STRB12M	STRB12M	MRKR2M	STRBDIS1M
25	IN11P	STRB3P	STRB21P	STRB21P	MRKR3P	STRB2P
26	IN12P	STRB4P	STRB22P	MRKR1P	MRKR4P	STRBDIS2P
27	IN11M	STRB3M	STRB21M	STRB21M	MRKR3M	STRB2M
28	IN12M	STRB4M	STRB22M	MRKR1M	MRKR4M	STRBDIS2M
9	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD
10	INCOM	INCOM	INCOM	INCOM	INCOM	INCOM
19	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD
20	INCOM	INCOM	INCOM	INCOM	INCOM	INCOM
29	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD
30	INCOM	INCOM	INCOM	INCOM	INCOM	INCOM
32	5VP	5VP	5VP	5VP	5VP	5VP
33	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD	SHIELD
31	OSC	OSC	OSC	OSC	OSC	OSC
34	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE
35	OUTPWR	OUTPWR	OUTPWR	OUTPWR	OUTPWR	OUTPWR
36	OUT1	HSCOUT1	HSCOUT1	HSCOUT1	HSCOUT1	HSCOUT1
37	OUT2	HSCOUT2	HSCOUT2	HSCOUT2	HSCOUT2	HSCOUT2
38	OUT3	HSCOUT3	HSCOUT3	HSCOUT3	HSCOUT3	HSCOUT3
39	OUT4	HSCOUT4	HSCOUT4	HSCOUT4	HSCOUT4	HSCOUT4
40	OUTCOM	OUTCOM	OUTCOM	OUTCOM	OUTCOM	OUTCOM

Appendix D Module Specifications

This appendix provides specifications for the Series 90-70 High Speed Counter.

Specifications for the High Speed Counter

General:			
Module Operating Voltage	5 VDC (from backplane)		
Module Current Drain	1A + (10 mA x number of ON outputs) + (1.6 x encoder current)		
Maximum Count Rate			
Types A - D, and Type E in Up/Down mode	200 KHz		
Type E in A Quad B mode	800 KHz		
Output Points	Powered by user supplied 5V, or 10 to 30 VDC		
LEDs	MODULE OK and O1 - O4 (Output circuit. status)		
Input and Output Isolation			
Peak (1 second)	1500 volts		
Steady Status	30 V AC / DC		
Inputs			
Voltage Range			
TTL	5 VDC		
Non-TTL	10 to 30 VDC		
Magnetic Pickup (I1 to I4 only)	400 mV		
Input Thresholds (I1 to I12)	*TTL*	*Non-TTL*	*Magnetic Pickup*
V_{on}	1.4V	8.0V	400 mV
V_{off}	0.8V	5.0V	200 mV
Encoder Power	5 VDC, 500 mA @40°C (104°F), 300 mA @60°C (140°F)		
Input Filter Delay			
IN1 to IN8	10 ms or 2µs selectable		
IN9 to IN12	2µs		
Input Impedance	6000 ohms		
Input Hysteresis	250 mV typical		
Input Cable	Shielded cable recommended Maximum length: 30 meters (100 feet)		

Outputs	
Output Type	Positive Logic, optically isolated
Maximum Supply Voltage	30.0 VDC
Maximum Output Current at 60°C (140°F)	1.0 A for each output using 10 to 30 VDC supply
Output Current using 5 VDC supply	20 mA typical
Inductive Load Clamp Voltage	–8.0 V typical
OFF State Leakage Current	10 µA for each output
Output Response Time	
Type A - D, Type E Slow Response	300µs typical 650µs worst case
Type E Fast Response	*24 Volts*: On: 7µs typical 10µs worst case Off: 56µs typical *5 Volts* On: 10µs typical 15µs worst case Off: 63µs typical
Output Response Variation	
Slow Response	650µs worst case
Fast Response	1 µs worst case
Output Protection	5.0 A fuse (5x20mm replaceable) common to all outputs
VME	System designed to support the VME standard C.1

† Refer to GFK-0867B, or later for product standards and general specifications.

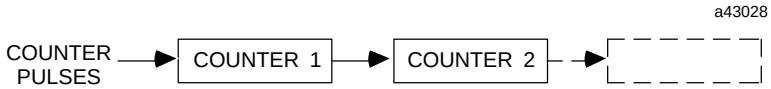
Appendix E Application Examples

This appendix contains descriptions of several typical applications using the Series 90-30 High Speed Counter. These application examples are:

- Counter Cascading
- Monitoring and Controlling Differential Speeds
- Direction-Dependent Positioning
- RPM Indicator
- Tolerance Checking
- Measuring or Comparing Pulse Rates
- Measuring Pulse Time
- Measuring Total Material Length
- Material Handling Conveyor Control
- Timing Pulse Generation
- Digital Velocity Control
- Dynamic Counter Preloading
- Carousel Tracking

Counter Cascading

Type A counters can be cascaded to accumulate greater count values than are possible with a single 2-byte counter. This can be accomplished by using the preset output of one counter for the count input of the next as shown below.

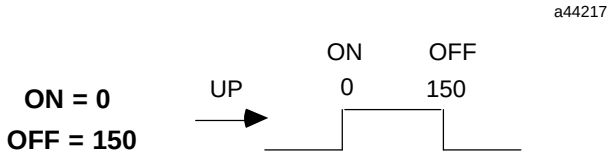


For example, if a 4-byte Up Counter is required, use two counters configured for the UP direction and:

1. Set the Count Limits for both counters at their maximum values:

   LOW = –32768 and HIGH = +32767

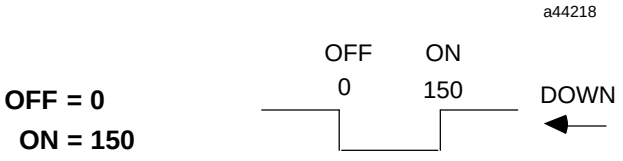
2. Set the output preset for counter 1 at:



3. Connect counter 1 output to the counter 2 input.

4. Connect the count pulse stream to the counter 1 input.

Similarly, Down Counters can be cascaded by configuring all counters for the Down direction, setting the limits at the maximum values and reversing the output presets. For example:



Monitoring and Controlling Differential Speeds

Many industrial applications require machines such as cutters, conveyors, or nip rolls to operate at precise differential speeds. The Type C counter, which could be used with a minimum of controller support is most suited for this application. Type A or Type B counters could also be used with the aid of a controller.

The pulses representing the speed of each machine can be separately fed into the plus and minus loops of the Type C counter. The accumulator will automatically track and indicate the difference in speed of the two machines. The sign of the accumulator value will indicate which pulse stream count is greater and the accumulator will indicate the total accumulated count difference. The Counts / Timebase register (CTB) will indicate the present rate difference and its sign indicates which is greater.

Depending on the count signal types, each channel of the counter can be independently programmed to operate in any of its three modes:

1. Pulse / Direction
2. Up / Down
3. A quad B

The sign (+ or –) and magnitude of the deviation from the desired difference can be used as feedback to provide automatic control for the speed regulation of the machines.

Direction-Dependent Positioning

Features Used :	Counter Type:
Single–Shot Mode	B
Preload Inputs	
Preset Outputs	

Some applications require direction-dependent positioning. An example is an operation where a crane on tracks has to perform certain maneuvers while traveling 100 feet in one direction and different ones while traveling 100 feet in the reverse direction.

This example uses the Type B configuration with two counters configured to operate in the A Quad B mode. Both counters should be driven by the same A Quad B signals and connected so they count in opposite directions when the crane is moving, as shown in Figure B-3 (Example of Terminal Connections).

The counter operating mode, limits and preload value can be set so that the preset outputs are direction sensitive. In this example, this is done by using the single-shot mode and preloading Counter 2 so that it only counts when the crane is moving in the reverse direction (right-to-left).

The counters are both preloaded at the start point and Counter 1 will count up from 0 to 100 for the left-to-right direction, and count down for travel in the right-to-left direction. Counter 2 will count up from (–100 to 0) only when the crane travels from right-to-left.

Table E-1. Counter Configurations

Parameter	Configuration
Counter Type	Type B (two counters)
Counter Operating Mode	A Quad B
Count Mode	one-shot (both counters), (non-continuous)
Counter 1 Preload	0
Counter 2 Preload	–100
Counter 1 Limits	0 to 100
Counter 2 Limits	–100 to 0

Table E-2. Operating Count Directions

Counter Number	Crane Direction	Count Direction
Counter 1	→	UP
Counter 2	→	Not counting
Counter 1	←	DOWN
Counter 2	←	UP

In this example, Counter 1 is configured with a preload value of 0. An ON condition for Preset 1 is selected which will turn on a loading device when the crane has traveled 75 feet to the right. Preset 2 (also for Counter 1) is selected to come on when the crane has traveled 100 feet to the right.

The direction of travel is reversed at the Stop point, and as the crane travels back from right-to-left, the ON Preset 1 of Counter 2 activates an unloading device when the crane has traveled 40 feet to the left (ON Preset is –60).

Finally, Preset 2 of Counter 2 turns its output on when the crane has traveled 75 feet to the left (ON Preset is –25).

The desired operation of the crane in this example is shown in the following figure.

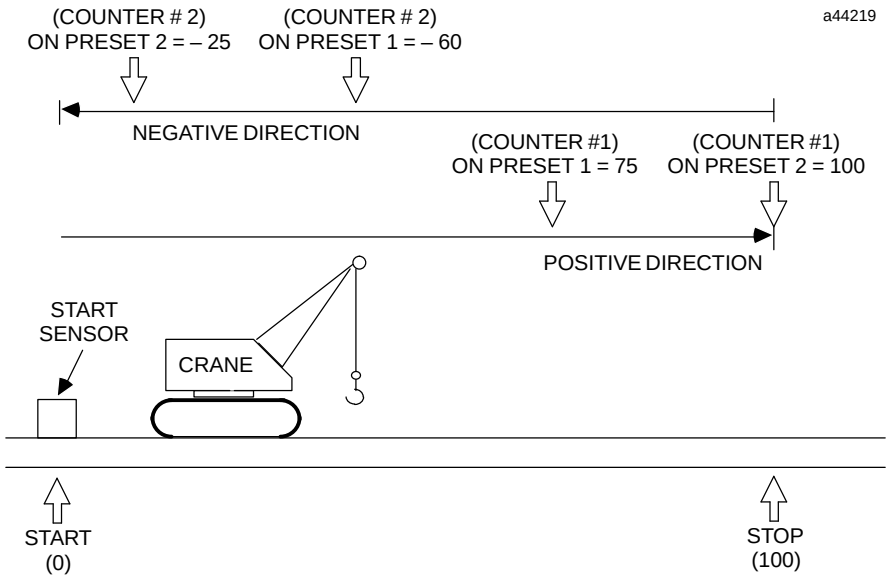


Figure E-1. Example of Direction-Dependent Sensing

OutputConditions

Counter1:	
Output 1	ON for Counter 1 y 75
	OFF for Counter 1 t 75
Output 2	ON for Counter 1 y 100
	OFF for Counter 1 <100
Counter2:	
Output 3	ON for Counter 2 v –60
	OFF for Counter 2 >–60
Output 4	ON for Counter 2 v –25
	OFF for Counter 2 >–25

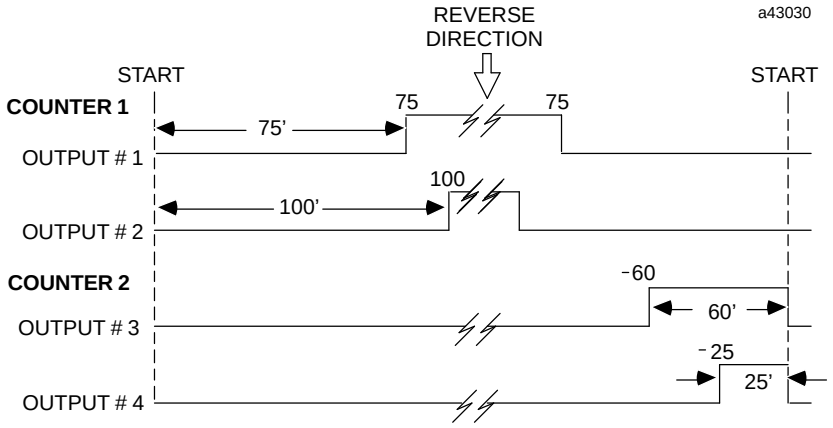


Figure E-2. Output Timing Conditions Example

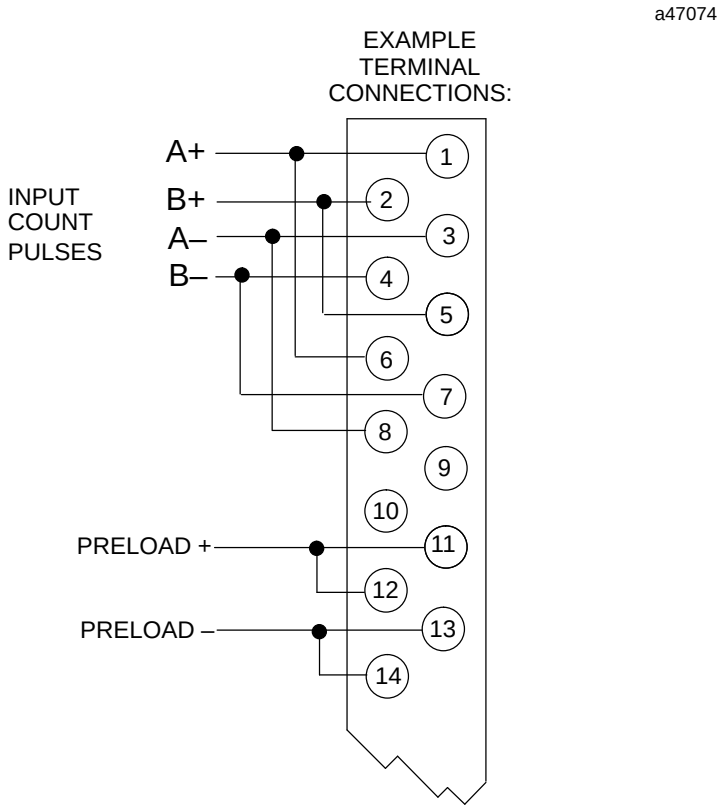


Figure E-3. Example of Terminal Connections

RPM Indicator

Feature Used:	Counter Types:
Counts/Timebase Register	A, B, C, D

The High Speed Counter can be used as a position / motion indicator when connected to a feedback device (such as an encoder) that is coupled to a rotary motion. RPM indication can be obtained directly from the counter's Counts / Timebase register (CTB) or derived from it by a simple calculation.

The RPM is given by:

$$RPM = \frac{CTB}{PPR} \times \frac{1}{T}$$

where: CTB = counts/timebase reading from the counter
PPR = pulses/revolution produced by the feedback device
T = timebase expressed in minutes

Note that if 1 / T divided by PPR is some integer power of 10, then the CTB register gives a direct reading of RPM with an assumed decimal placement. Longer timebase settings will give better RPM resolution. This is illustrated in the following examples.

Example 1

If feedback produces 1000 pulses / revolution, CTB reading = 5212, and the timebase is configured for 600 ms:

then T = 600 ms Ï 60000 ms / min = .01 and 1 / T = 100
RPM = 5212 Ï 1000 x 100 = 521.2

CTB reading is RPM with .1 RPM resolution.

Example 2

Assume the same conditions as example 1, except the timebase is now set to 60 ms, which gives

T = 60 Ï 60000 = .0001 and 1 / T = 1000.

Since the motion is turning at the same speed as in example 1, the CTB reading now equals 521,

and RPM = 521 / 1000 x 1000 = 521.

CTB reading is now RPM with 1 RPM resolution.

Tolerance Checking

Features Used:	Counter Type:
Strobe Inputs with Positive/Negative Strobe Edge Configuration	B

Parts can be measured by a counter for tolerance checking. This can be accomplished by coupling a pulse feedback device to the transport conveyor to provide count inputs representing increments of movement to the measuring counter.

For this example, a Type B counter is used and the same part sensing signal is connected to both strobe inputs. The first strobe input is configured to be active on the leading edge and the second on the falling edge. Then as each part passes through the sensor, its length is indicated by the difference between the two strobe register readings. Multiplying the difference by the known distance represented by each pulse gives the length in measurement units for comparison against the allowable tolerance. Parts out of tolerance may be marked or diverted into a separate reject storage area.

An illustration of this application is shown below along with an example of field connections to the High Speed Counter's terminal board.

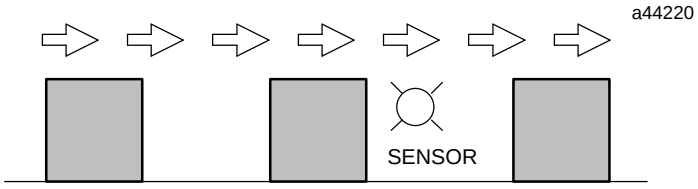


Figure E-4. Example of Tolerance Checking

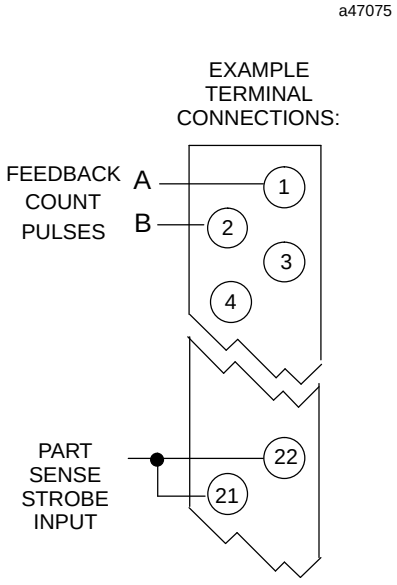


Figure E-5. Terminal Connections

Measuring or Comparing Pulse Rates

The High Speed Counter can accurately measure a pulse rate or compare the rates of two pulses. If the measured pulse rate will be less than 1 KHz, one Type A counter can be used, as described in example 1, below. If the measured pulse rate may exceed 1 KHz, the High Speed Counter should be configured for Type B counter operation, and set up as described in example 2.

Using a Reference Pulse

To accurately measure a pulse rate, a pulse stream with a known frequency of up to 200 KHz is used as a reference. The reference frequency should be at least 10x the pulse rate to be measured.

The reference pulse can come from an external source, or from the counters own oscillator output (OSC). If the OSC output is used, it can be configured for a frequency up to 200 KHz (oscillator divider = 5). To use the OSC output, the counter must be configured for TTL-level Counter Input Threshold voltage (page 3-7). The OSC output can be jumpered directly to the counter input terminal.

Example 1: Measuring a Pulse Rate Less Than 1 KHz

For this application, configure the High Speed Counter for Type A counter operation. Configure the Strobe Effect feature for *Strobe Then Preload.* Configure a Preload value of 0, and configure the Count Direction to be UP.

Connect the reference pulse to the Count Input. Connect the pulse to be measured to the Strobe input.

As each measured pulse is received, the number of reference pulses received is captured in the Strobe Register, and the Accumulator is preloaded back to 0. The Strobe Register always indicates the number of known-frequency pulses between each measured pulse, and its instantaneous rate can easily be calculated.

Example 2: Measuring a Pulse Rate Over 1 KHz

For this application, the High Speed Counter should be configured for Type B counter operation. The Strobe Linkage feature should be configured to *ACC2* (linked) (page 4-12). Apply the pulse rate to be measured to the input of Counter 2, as illustrated.

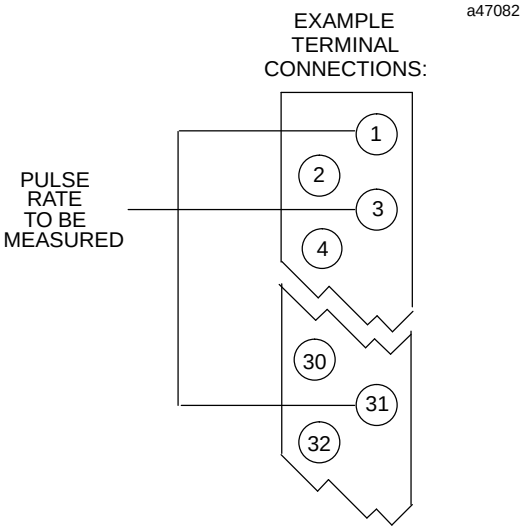
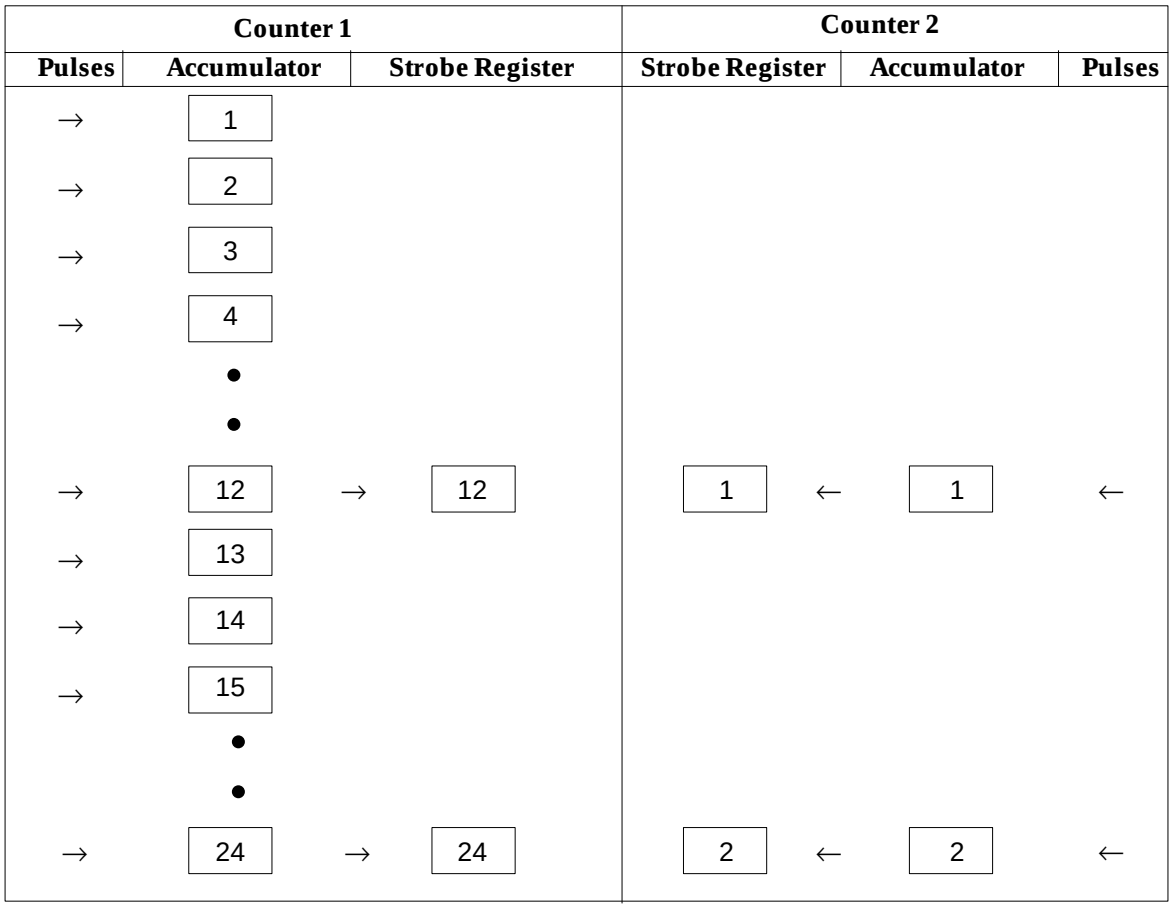


Figure E-6. Example of Terminal Connections

At the rising edge of each measured pulse, the counter will:

1. Count the #2 Counter up (or down).
2. Transfer the contents of Counter 1 into Strobe Register 1.1.
3. Transfer the contents of Counter 2 into Strobe Register 2.1.

Steps 2 and 3 occur simultaneously, so Strobe Register 2.1 always contains the number of measured pulses and Strobe Register 1.1 always contains the corresponding number of measuring pulses to within Ç 1 count.



The counter automatically transmits this Strobe Register data to the CPU. The application program should:

1. Find the difference between two successive sets of Strobe Register values. In the illustration above,
   A. for Strobe Register 1.1: 24 –12=12
   B. for Strobe Register 2.1: 2 –1= 1
2. Divide the number of pulses from Strobe Register 1.1 by the number of pulses from Strobe Register 2.1. This will give the ratio between the pulse rates. In the example, the ratio is 12 to 1.
3. To find a measured pulse rate, the program should divide the reference pulse rate by the number found in step 2. If the reference from the OSC output were 200 KHz, the measured pulse rate for the example would be 16.7 KHz (200 Ï 12).

Measuring Pulse Time

Features Used:	Counter Type:
Ref Osc Input	B
Strobe Inputs	

ON / OFFtime of input pulses can be accurately measured using the High Speed Counter. This can be done by configuring the Ref Osc input into Counter 1 and using the two Strobe inputs to capture the counter value on each of the input pulse edges.

For example, assume that an input pulse needs to be measured to the nearest 0.1 milliseconds; configure the High Speed Counter as follows:

```
Counter:  Type B
  Osc Freq Div = 66 (10 kHz)
  Osc IN 1 = ON (1)

For Counter 1:
  Mode = Continuous
  Strobe 1 Edge = Pos
  Strobe 2 Edge = Neg
```

Connect the pulse signal to both Strobe inputs. When the signal occurs, its duration (in tenths of ms) is now given by [Strobe Reg 2 – Strobe Reg 1] for positive going pulses or [Strobe Reg 1 – Strobe Reg 2] for negative going pulses.

Note that if the pulse spans the counter rollover point, the calculation becomes more complex, therefore it may be desirable to preload the counter to 0 shortly before the pulse is measured.

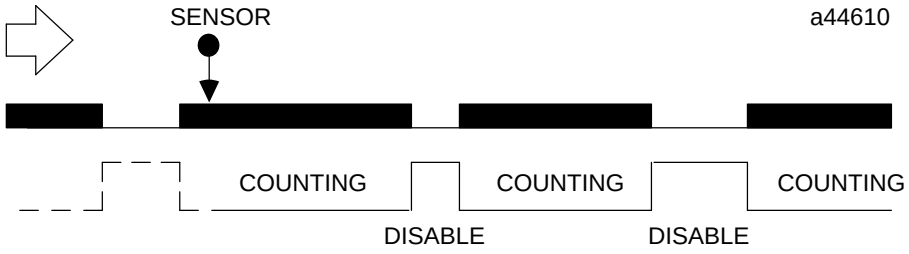
If only a positive-going pulse is measured, it could also be connected to the preload input. The Strobe Reg 2 reading would now give the pulse length directly.

Measuring Total Material Length

Features Used:	Counter Type:
Disable Input	B

The total length of multiple pieces of material, such as plate glass, plastic strips, or lumber, can be measured with the High Speed Counter.

This application uses an encoder geared to a transport conveyor to provide the count input increments, and a sensor to detect material as it passes.



The High Speed Counter should be configured for Type B counter operation.

Connect the encoder to the counter's Count Input. Connect the sensor to the Disable Input.

Count inputs from the encoder will increment the Accumulator only while a piece of material is passing through the sensor. The total length of all pieces will be accumulated until the counter is reset (Preloaded) for the start of a new batch. The application program can convert the count units from the accumulator to the actual units of length being measured.

Material Handling Conveyor Control

Features Used:	Counter Type:
Preset Outputs	B

When transported material must be stopped momentarily for inspection or modifications, the High Speed Counter's Preset outputs can control conveyor slowdown and stop points.

Use an encoder geared to the transport conveyor to provide the count input increments. Use a sensor to detect material as it passes on the conveyor.

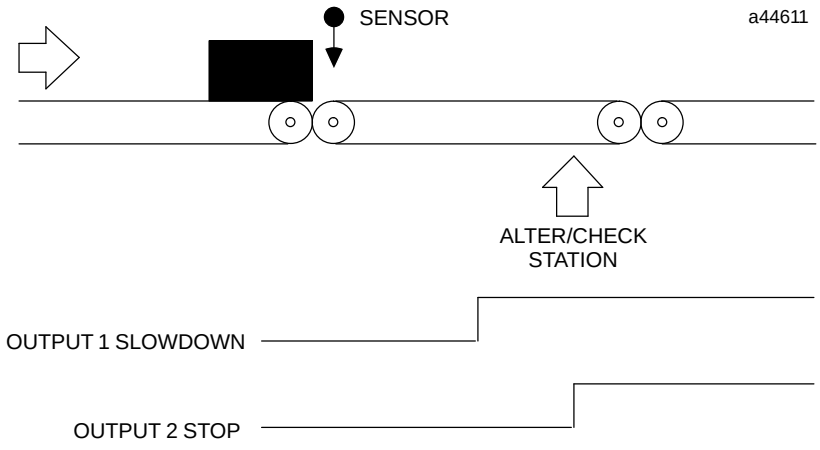
Determine where the material should begin to slow down, and where the material should stop. Find out how many encoder counts are equivalent to each of these two distances.

The High Speed Counter should be configured for Type B counter operation.

Configure Preset Output 1 to turn on at the slowdown point, by entering the number of counts from the sensor to the point where slowdown should begin.

Configure Preset Output 2 to turn on at the stop point, by entering the number of counts from the sensor to the inspection station.

Connect the sensor to the Preload Input of the counter to restart the counter at 0 for each piece of material that passes (only one piece can be between the sensor and the stop point in this configuration).



Timing Pulse Generation

Features Used:	Counter Type:
Ref Osc Input	A
Preset Output	

Applications requiring an accurate timing pulse can use the High Speed Counter to generate the pulse at the required frequency. The specified pulse width will be accurate to 0.5 msec of resolution.

Assume that a pulse of 50 msec duration is needed every 1/2 second. The High Speed Counter could be configured as follows to give the desired pulse output.

Counter type A

Oscillator Frequency Divider (N) = 100 (10kHz)

Oscillator Frequency Input 1 = ON (1)

For counter 1:

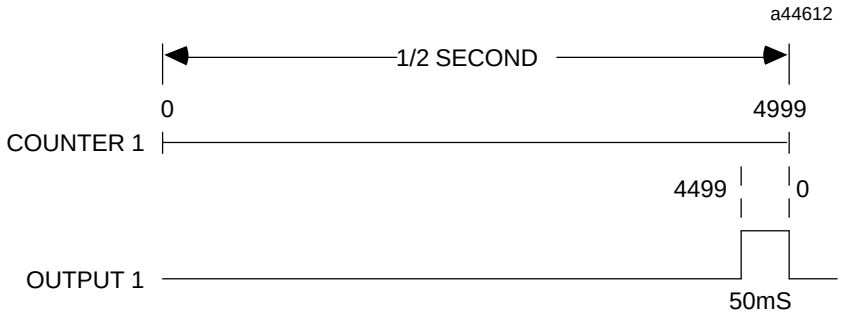
mode = continuous

high limit = 4999

low limit = 0

On Preset = 4499

Off Preset = 0



The counter's upper limit of 4999 represents 5000 counts, the number of counts in 1/2 second at 10kHz. (For this example, the Oscillator Frequency could also have been set to 1kHz. If that had been done, the upper limit would have been 499.)

Setting the lower limit to 0 establishes the counter start point for each output pulse period. The On Preset, 4499, determines that 4500 counts will pass before the beginning of the output pulse. Setting the Off Preset to 0 turns off the output pulse when the Accumulator reaches 5000 counts.

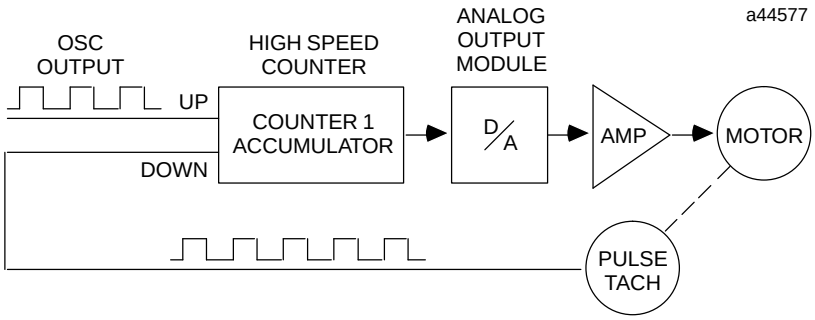
Digital Velocity Control

Features Used:	Counter Type:
Ref Osc Input	B
Up/Down Mode	

The High Speed Counter, together with an Analog Output module and a drive amplifier, can be used to provide accurate motor velocity control. The commanded velocity is generated by connecting the internal oscillator to the up count input of Counter 1.

The OSC input (or an external oscillator) provides a steady counting pulse to the up count input. The output of the counter provides the accumulator count value to the CPU. This data can be transferred by the CPU to an analog output module. An output from this module, in turn, controls the amplifier driving the motor.

During system operation, the motor's velocity can be changed by changing the frequency of the OSC output.



A pulse tachometer is connected to the block's down count input. This tachometer provides count pulses that are fed into the down count input of the same counter. As a result, the counter Accumulator reaches a stable value when the motor is turning at the commanded velocity.

Dynamic Counter Preloading

Feature Used:	Counter Type:
Home	C

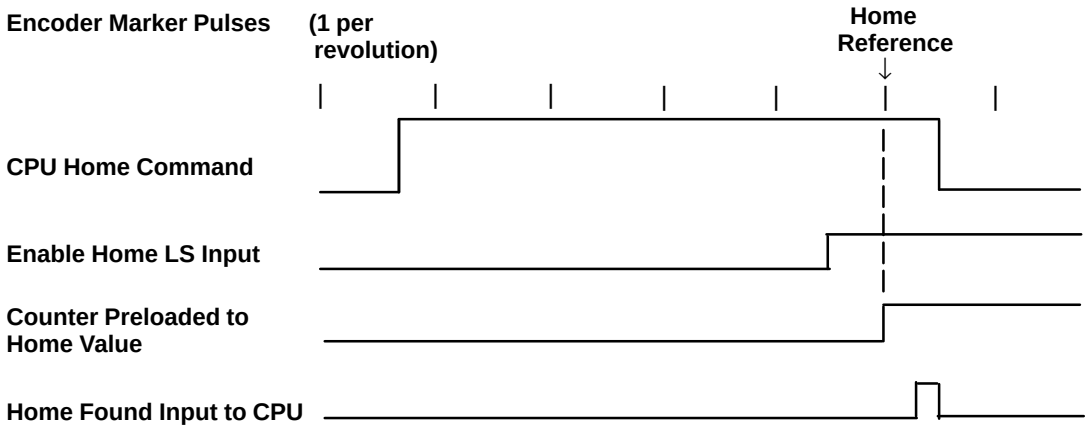
Applications using a High Speed Counter to track the position of a material conveyor or machine slide may need to be preloaded accurately at a given reference point while in motion. Simply connecting a limit switch to the counter's Preload Input does not give repeatable, accurate results because errors are introduced by:

1. Variations in the actuation point of the limit switch and
2. Preload Input Filter delay when actuated at different speeds.

For accurate repeatability, the Home feature of the Type C counter configuration should be used. This application requires a marker pulse (usually 1 per revolution) from the position feedback device (encoder). The limit switch should be placed so that it will be encountered approximately halfway between marker pulses. When the limit switch is reached, the next marker pulse causes the High Speed Counter to preload the Accumulator with the desired value. The limit switch should be connected to the High Speed Counter's Enable Home input.

The operation is as follows:

1. As the conveyor or slide moves toward the reference position, the CPU issues the Home Command (by setting output bit 14 to the High Speed Counter).
2. The Enable Home limit switch is actuated. This informs the High Speed Counter that the next marker pulse will be the reference marker.
3. When the next (reference) marker is reached, the High Speed Counter automatically transfers the Home value to the counter Accumulator.
4. The High Speed Counter informs the CPU that Home position has been found by setting input status bit 4.
5. The CPU may then clear the Home Command (output bit 14), causing the block to remove the Home Found indication.



Carousel Tracking

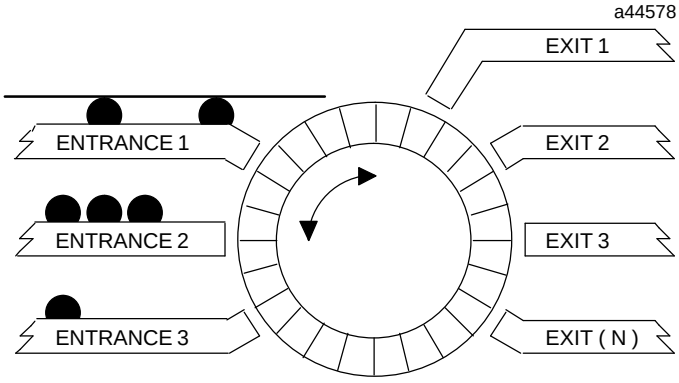
Features Used:	Counter Type:
Home Inputs	C
Strobe Inputs	
Continuous Mode	

Items stored in a rotating carousel can be tracked and retrieved using a High Speed Counter. A feedback device coupled to the carousel rotation can be used to provide up / down count inputs. The counter limits are configured so that the increments produced by one complete revolution of the carousel cause one full cycle of the counter.

Type C counter configuration is best for this application, since it provides a homing capability. The homing capability makes it possible to synchronize the counter with the carousel position at a defined home location after powerup. From then on, any rotation of the carousel is tracked by the counter. Since the relative location of all entrance and exit points to the home position is known, the CPU can record the pocket location of each item entering the carousel. It can command any pocket to any exit for item retrieval.

If there are up to 3 entrance points, a different Strobe Input can be used to indicate when a pocket is loaded from each entrance. When the CPU detects the Strobe Set flag, it can record the pocket position into a memory table and mark it full. (The CPU records the pocket position by reading the value from the Strobe Register, then adding or subtracting the entrance offset from the home location.)

To retrieve an item from a particular exit, the CPU can locate the nearest full pocket to that exit, and generate the required rotation command to the carousel.



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